Applied Mechanical Tensile Strain Effects on Silicon Bipolar and Silicon-Germanium Heterojunction Bipolar Devices

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Applied Mechanical Tensile Strain Effects on Silicon Bipolar and Silicon-Germanium Heterojunction Bipolar Devices

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SUMMARY

This work investigates the effects of post-fabrication applied mechanical tensile strain on Silicon (Si) Bipolar Junction Transistor (BJT) and Silicon-Germanium (SiGe) Heterojunction Bipolar Transistor (HBT) devices. Applied strain effects on MOSFET transistors are being heavily explored, both in academia and industry, as a possible alternative to dimensional scaling. This thesis focuses on how strain affects Si BJT and SiGe HBTs, where tensile strain is applied after the Integrated Circuit (IC) fabrication has been completed, using a unique mechanical method. The consequence of both biaxial and uniaxial strain application has been examined in this work.

Chapter I gives a short introduction to the scope of this work, the motivation for conducting this research and the contributions of this experiment.

Chapter II entails a brief discussion on Si bipolar and SiGe heterojunction bipolar device physics, which are key to the understanding of strain induced effects.

Chapter III provides a thorough summary of the current state of research regarding applied strain, also known as Strain Engineering. It covers different types, orientations, and application techniques of strain.

Chapter IV, highlights the details of this experiment, and also presents the measured results. It is observed that for this particular method of biaxial tensile strain application, the collector current (I_C) and current gain (β) degrades for both Si BJT and SiGe HBT. Base current (I_B) decreases in Si BJT, though it increases for SiGe HBT after strain. Little or no change is noticed in the dynamic or *ac* small-signal characteristics like unity-gain cutoff frequency (f_T) and base resistance (r_{BB}) after strain. Uniaxially strained SiGe HBT samples showed similar results as the biaxial strain. This chapter also attempts to explain the origin of these strain induced changes.

Chapter V, summarizes the finding of this experiment, and concludes the thesis with some future directions for this research.

CHAPTER I

INTRODUCTION

1.1 Motivation

Transistors, the heart of modern Integrated Circuits (IC), have come a long way from its first inception. Innovations in the fabrication technology has accelerated the aggressive scaling of transistor geometries. In 1965, Gordon Moore made the prediction that the number of transistors on a chip will roughly double every two years, famously know as Moore's Law. Advancement in process and device technologies have fueled the down scaling of transistor geometries, and Moore's law has prevailed for 40 years. International Technology Roadmap for Semiconductors (ITRS) predicts CMOS scaling to and beyond the 22-nm technology node which requires a physical gate length of 9-nm or less [1]-[3]. However, as the CMOS devices are shrinking, fundamental physical barriers are becoming more and more important. With traditional or classical MOSFET structures, addressing issues like leakage current, power dissipation, defect density and reliability are critical for maintaining device, and in turn overall circuits and systems performance. As a result, alternatives to dimensional scaling are being heavily explored for enhanced device and circuits performance. Different transistor topologies and materials are being investigated. From a new material research perspective, metal gate or high-k gate dielectric materials (like HfO_2 [4]) and self-aligned silicides (salicide) are two main areas of focus [5]. The other trend has been to search for novel transistor architectures, like multi-gate transistors [2]-[3], non-planar structures [6], different variations of Silicon-on-Insulator (SOI) [7] or FinFETs [8]-[9].

One other transport enhanced transistor structure is Strain-Si, which has gained tremendous popularity and already is a viable commercial technology. It is considered as a capable alternative to dimensional scaling, and believed to delay the innovation of other novel transistor structures, that are still in research phase, by a substantial period [10]. Several research groups, wafer fabrication foundries and integrated circuit manufacturers have reported the enhancement of device performance in terms of higher drive current (I_D) in CMOS devices [11]-[12]. These publications show an increase in drain current (I_D) by a significant amount, associated with higher carrier mobility. This translates to significant reduction (about 35%) in power dissipation at the same performance or speed, or an increase in performance at similar power consumption [11].

While the silicon CMOS industry is already leveraging such strain-induced enhancements, very few papers have reported the effects of strain on Si bipolar transistors (BJT) or SiGe heterojunction bipolar transistors (HBT) [13]-[15]. Here comes the motivation to investigate the effects of applied strain on Si BJT and SiGe HBTs. Si BJT and SiGe HBTs have been scaled down as well, with superior performance and different vertical profile than the previous generations [16]. The objective of this work is to investigate the potentials of strain engineering in Si BJT and SiGe HBT in achieving higher performance out of an otherwise lower performance technology or device.

1.2 Contributions

This work presents the results of mechanical uniaxial and planar biaxial tensile strain applied to Si bipolar transistors (BJT) or SiGe heterojunction bipolar transistors (HBT). There are different methods of inducing strain on transistors, which are described in detail in Chapter III. This thesis examines the effects of tensile strain, applied post-fabrication in a particular mechanical manner on bipolar devices. The technique used for strain application in this experiment, is first of its kind on bipolar devices, as reported in technical literature. The effects of biaxial planar strain on bipolar and heterojunction bipolar devices, along

with CMOS, have been presented on Silicon Monolithic Integrated Circuits in RF Systems conference on September, 2004. The presentation was awarded as the runner up in the 'Best Student Paper' category. An elaborated version of the results of biaxial strain effects, titled as "The Effects of Mechanical Planar Biaxial Strain in Si/SiGe HBT BiCMOS Technology" is currently in press for publication at *Solid-State Electronics*. This thesis work can be used as a background study of the possibilities of bipolar/heterojunction bipolar device performance enhancements through strain.

CHAPTER II

BACKGROUND CONCEPTS

2.1 Introduction

In order to understand how strain application can affect the device performance in Si BJT or SiGe HBT, a thorough knowledge of their process technologies, device physics and carrier transport mechanism is crucial. This chapter lays down the basic foundation of bipolar and heterojunction bipolar devices, specially the process, technology, physics and performance of Si BJT and SiGe HBT.

2.2 Fundamentals of Bipolar Junction Transistor

Bipolar junction devices, as the name suggests, involve the movement of two types of carriers, namely electron and holes. The transport properties of minority carriers in the base region (electrons and holes for npn and pnp type devices respectively) are of greatest interest. In this work, we will focus on npn type bipolar devices only. The schematic cross section of a typical npn planar bipolar transistor is shown in Figure 1.

A bipolar junction transistor is often viewed as two back to back pn junction devices with a very thin or narrow base. The narrow base width, compared to the minority carrier diffusion length, guarantees the current flowing action in the BJT. For an npn device in forward active mode of operation, electrons are injected into the base from emitter through the forward biased EB (Emitter-Base) junction, and constitute I_{En}, the main component of emitter current I_E. These electrons diffuse across the base, and most of those are swept or collected by the reversed biased CB (Collector-Base) junction into the collector (causing I_{Cn}). Some of the holes from the p-type base travel to the n-type emitter region through EB junction, which gives rise to I_{Ep} (or I_{B1}), the major part of base current I_B. The other

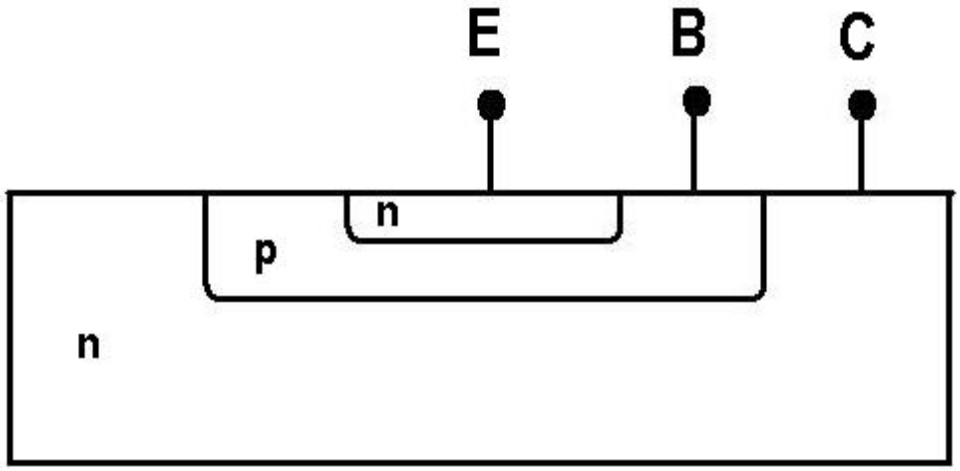

Figure 1: Cross section of a simple npn BJT.

components of I_B are I_{B2} and I_{Cp} (or I_{B3}). I_{B2}, which is proportional to the minority electron charge in base, represents the flow of majority carrier holes from the base lead into the base, that recombines with the minority carrier electrons that are injected from the emitter but can not make it to the collector side. I_{Cp} is due to the thermally generated minority holes at the collector near the CB junction that drift into the base. This is the basic carrier transport mechanism in a an npn type BJT [17]-[19]. Figure 2 illustrates different current components of an npn BJT. The total emitter, collector and base currents in an npn BJT are described in terms of their components in the following equations.

$$I_E = I_{En} + I_{Ep} \tag{1}$$

$$I_C = I_{Cn} + I_{Cp} \tag{2}$$

$$I_B = I_E - I_C = I_{Ep} + (I_{En} - I_{Cn}) - I_{Cp} = I_{B1} + I_{B2} - I_{B3} \tag{3}$$

Some key performance parameters for a BJT can be derived from these component currents. One of these parameters are emitter injection efficiency (γ), that measures the number of electrons injected from the emitter compared to the emitter current, as shown in Equation 4 for an npn BJT.

$$\gamma = \frac{I_{En}}{I_E} = \frac{I_{En}}{I_{En} + I_{Ep}} \tag{4}$$

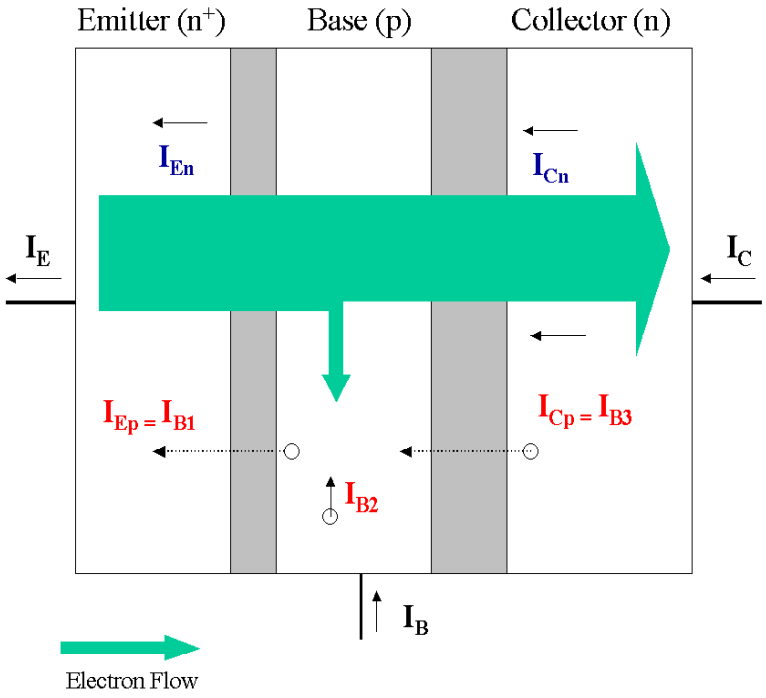

Figure 2: Emitter, collector and base current components of a npn BJT.

Equation 5 gives the base transport factor(α_T), which is the fraction of minority electrons injected from the emitter into the base that completely cross the narrow base width and enter the collector region.

$$\alpha_T = \frac{I_{Cn}}{I_{En}} \tag{5}$$

Clearly a large base transport factor indicates that a small portion of the injected carriers are recombined into the base, which is desired for higher performance. Another very important parameter is common emitter (CE) current gain (β) that is defined as the ratio of I_C and I_B.

$$\beta = \frac{I_C}{I_B} \tag{6}$$

These different currents along with the current gain (β) are very significant parameters for a bipolar device, and the effects of strain on these quantities will be an important part of this study. The collector current in a BJT is exponentially dependant on V_{BE}, as shown in Equation 7.

$$I_C = I_S e^{qV_{BE}/kT} \tag{7}$$

where the saturation current (I_S) for a npn BJT is given as

$$I_S = \frac{qAD_{nb}n_{io}^2}{N_{ab}^- W_b} \tag{8}$$

Here A, D_{nb} and n_{io}^2 refer to the area of EB junction, the minority electron diffusivity in the base and the square of the intrinsic carrier concentration respectively, whereas N_{ab}^- and W_b are the base doping and width correspondingly. D_{nb} is related to the electron mobility (μ_n) via Einstein's Equation (9)

$$\frac{D_{nb}}{\mu_n} = \frac{kT}{q} \tag{9}$$

Combining the above equations, the collector current can be expressed as

$$I_C = \frac{kTA\mu_n n_{io}^2}{N_{ab}^- W_b} e^{qV_{BE}/kT} \tag{10}$$

Electron mobility and intrinsic carrier concentration in the base of a BJT are of great importance, and how strain affects these metrics and in turn changes collector current will be discussed in chapter IV.

2.3 Si BJT and SiGe HBT: An Overview

The development of Integrated Circuits (IC) have played a major role in building the foundation of modern technological breakthroughs. Silicon (Si), being the material of choice for the transistors in ICs, is at the forefront of driving the information technology era. The abundance of Si, added with several other favorable features have made it a suitable semiconductor, from an economical and manufacturing perspective. One key benefit is the ability to grow high-quality dielectric (SiO_2) on Si by thermal oxidation or chemical vapor deposition (CVD). There are other advantages like higher yield and integration, high range of doping control (both n and p-type), excellent thermal and mechanical properties, easiness of etching and many more [16].

Of the two types of transistors, Si bipolar devices have certain advantages over Si CMOS devices, like faster switching speed, higher gain and larger current driving capability [19]-[20]. Si BJT, in particular is very suitable for analog circuits, whereas CMOS

is geared more towards digital, memory and VLSI applications [21], due to the low power dissipation and higher density. In specific applications, Si BJT is integrated with CMOS in the same process technology, known as Si BiCMOS technology, for achieving the best of both worlds. However, the advantages of Si are often mitigated by the fact that the mobility of electron and holes in Si are lower with respect to those of III-V compound semiconductors like GaAs or InP. This led to the innovation of first bandgap engineered Si transistor, known as SiGe hetorojunction bipolar transistor (HBT). SiGe HBT devices enjoy the benefits of Si BJT, with many other advantages. SiGe HBTs are well suited for high frequency applications, often rivalling the performance of the III-V semiconductors [16]. When combined with Si CMOS, termed as SiGe HBT BiCMOS technology, it is a true contender for System-on-Chip (SoC) design, with integration of digital, analog and RF circuits in the same wafer.

2.4 SiGe HBT: Fabrication, Device Physics and Performance

Heterojunction, as the name suggests is a junction between two dissimilar materials. In the context of HBTs, it refers to a junction between two dissimilar semiconductors. SiGe HBTs contain two heterojunctions, the n-Si/p-SiGe EB heterojunction and the p-SiGe/n-Si BC heterojunction. Traditionally for III-V HBTs, the emitter is composed of a wider band gap semiconductor than the base. This sets up a built-in voltage barrier (V_{bi}), which impedes the forward bias injection from the base to the emitter and gives rise to a high injection efficiency even when N_E is much smaller than N_B. However, in SiGe HBTs, the emitter is heavily doped with a moderately doped base.

2.4.1 Fabrication

The idea of bandgap engineering of Si via SiGe alloy is an old one, which dates back to 1951, at the time Shockley was inventing transistors [22]. But due to material growth

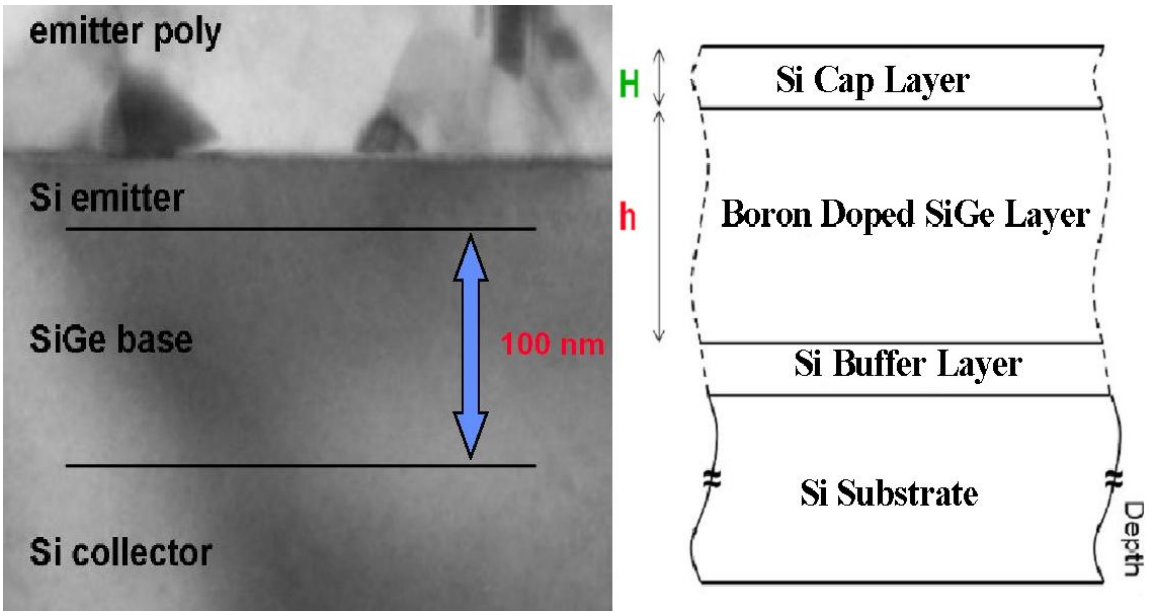

Figure 3: Cross sectional TEM displaying epitaxial SiGe film layers in a SiGe HBT (after [16]).

limitations, it took almost 30 years to successfully implement a reliable, stable and defect-free device quality SiGe film, that postponed the realization of SiGe HBTs. A typical SiGe film consists of a thin and undoped Si buffer layer, a boron-doped SiGe active layer, and a thin and undoped Si cap layer (Figure 3). The Si buffer layer ensures pure growth interface for the SiGe active layer, and also helps in breakdown voltage adjustment. The Si cap layer is used during oxidation in forming EB spacer for self alignment, and also for emitter out-diffusion [16].

The earlier SiGe epitaxy layers were grown using molecular beam epitaxy (MBE) [23]-[25] , but ultra-high vacuum/chemical vapor deposition (UHV/CVD) is the dominant technique [26]-[27]. Figure 4 depicts a SIMS doping and Ge profile for a representative first generation SiGe HBT. The Ge profile can have certain shape (box, triangle or trapezoidal), thickness and location with respect to the boron (B) base profile, and can be the determining performance parameter. Figure 5 exhibits the SEM profile of a second generation SiGe

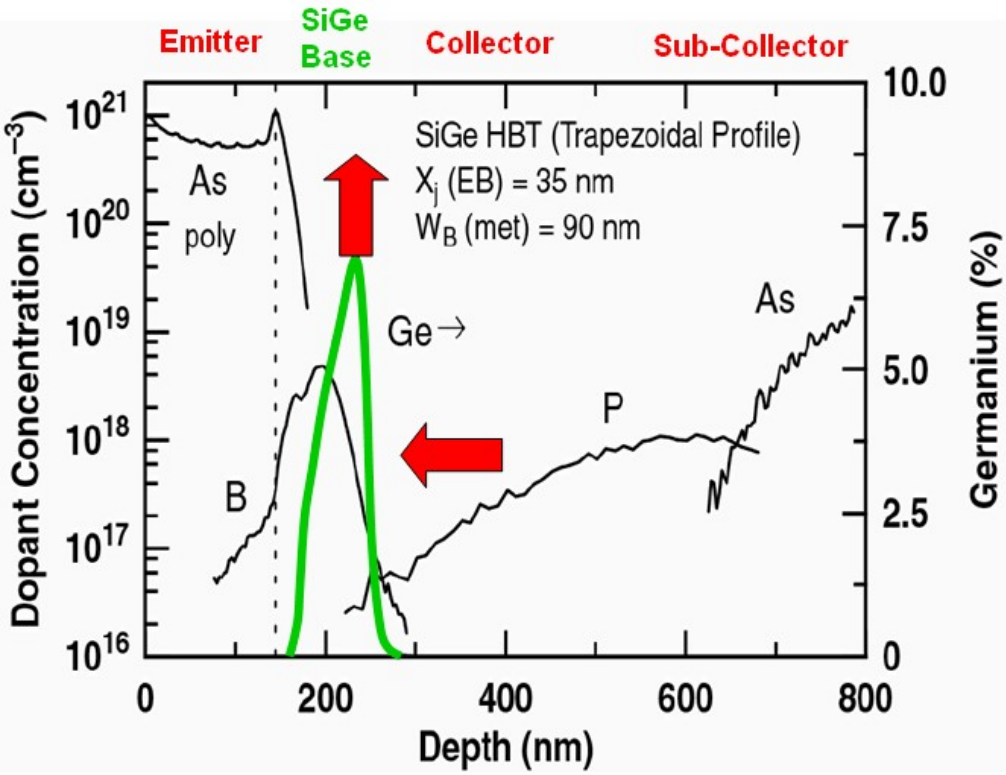

Figure 4: SIMS profile of a representative first generation SiGe HBT, exhibiting dopant concentration and Ge percentage (after [16]).

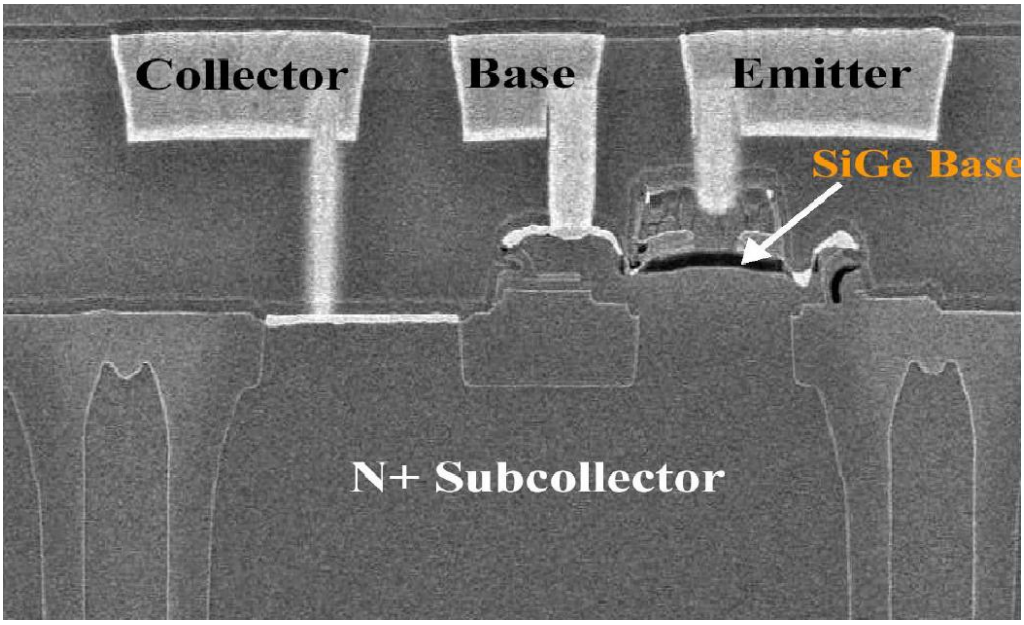

Figure 5: SEM profile of a representative second generation SiGe HBT (120 GHz peak f_T Process) (after [28])

HBT, whereas Figure 6 shows a schematic cross-section of the SiGe HBT. The pseudo-morphically grown SiGe needs to be thermodynamically stable, which is often relaxed as shown in Figure 7.

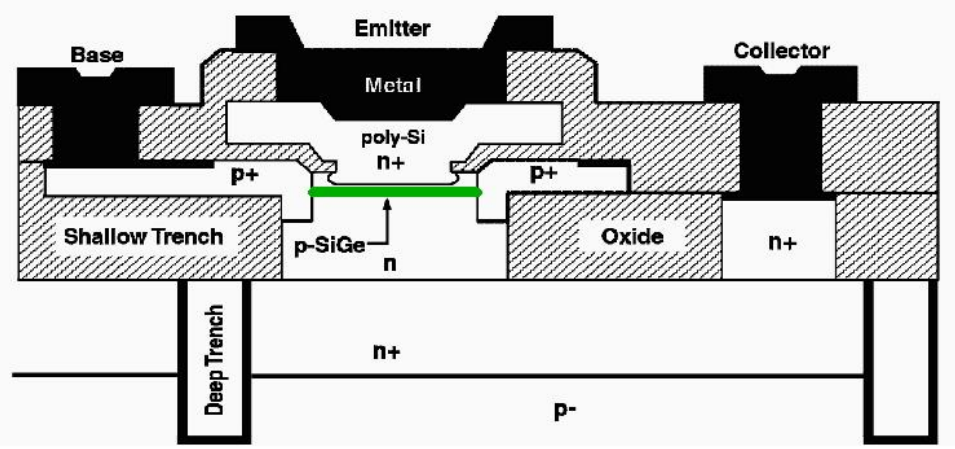

Figure 6: Schematic cross-section of the SiGe HBT (after [16]).

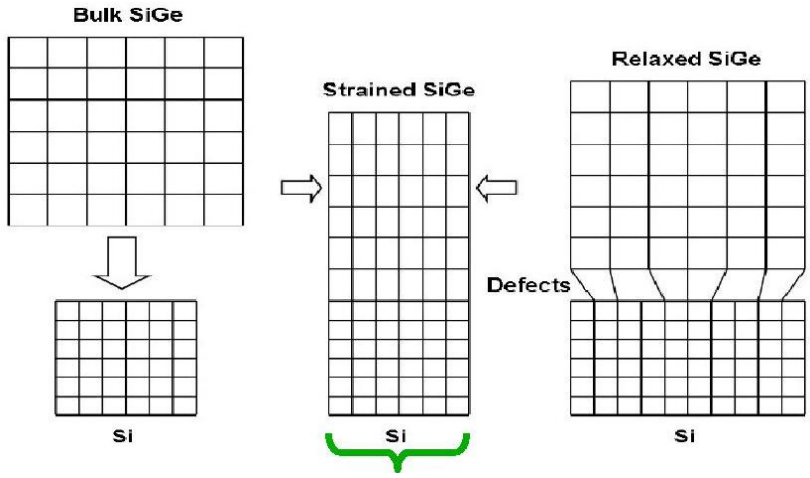

Figure 7: Schematic 2-D representation of both strained and relaxed SiGe on a si substrate (after [16]).

2.4.2 Device Physics and Performance

Si and Ge are both indirect energy gap semiconductors, but they have difference in their bandgap energies (Eg_{Si} = 1.12 eV and Eg_{Ge} = 0.66 eV). This accounts for a smaller

bandgap in SiGe than in Si, and compressive strain in SiGe base. The band alignment of SiGe HBT compared to pure Si also changes (Figure 8). For SiGe films, the valence band offset is dominant and approximately 74 meV/10% Ge content upto 30% Ge fraction [16], which eventually ends up in the conduction band. The perturbation of both the valence

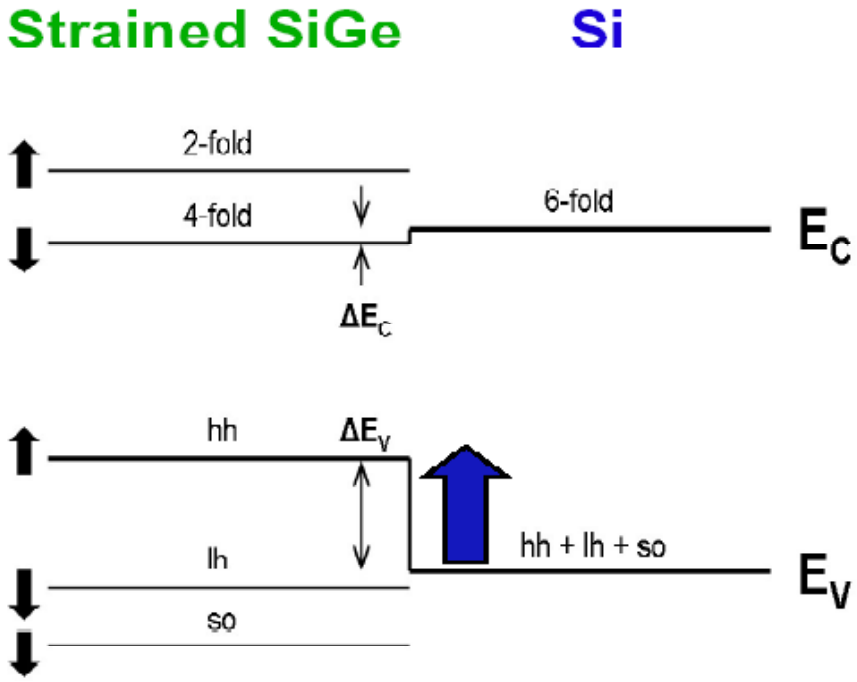

Figure 8: The band alignment of SiGe HBT grown on a Si substrate (after [16]).

and conduction band strongly degrades the density-of-states ($N_C N_V$), which can cause a reduction in the collector current. The distortion in the band edges also decrease the effective masses of the carriers (electron and hole), which counteracts the collector current reduction and increases the carrier mobility. Figure 9 shows the energy band diagram for a Si BJT and a graded SiGe HBT, both biased in forward active mode at low level injection. The bandgap reduction at the CB junction ($\Delta E_{g,Ge}(x = W_b)$) is larger compared to that of EB junction ($\Delta E_{g,Ge}(x = 0)$). The graded Ge across the neutral base induces a built-in electric field, which also improves the minority carrier transport. From a *dc* perspective, the presence of Ge reduces the voltage barrier for minority carrier electron injection into the base region from the emitter, and thus enhances collector current (I_C) and current gain

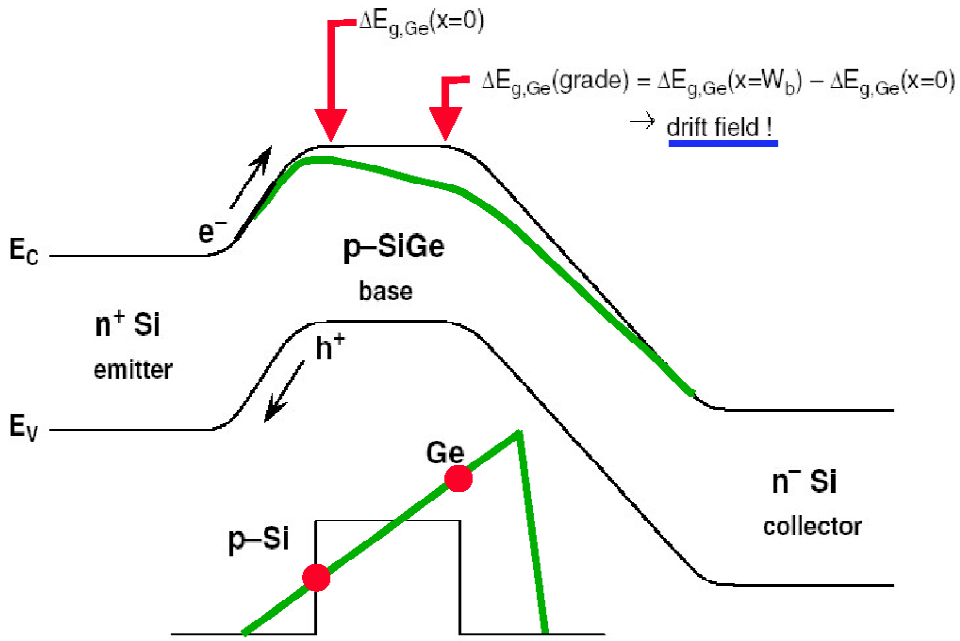

Figure 9: Energy band diagram for a Si BJT and a graded base SiGe HBT (after [16]).

(β). The generalized Moll-Ross collector current density equation [29] illustrates the Ge induced bandgap modification.

$$J_C = \frac{q\left(e^{qV_{BE}/kT} - 1\right)}{\int_0^{W_b} \frac{p_b(x)dx}{D_{nb}(x)n_{ib}^2(x)}} \tag{11}$$

where $p_b(x)$ is the base hole doping. The intrinsic carrier concentration in the SiGe HBT is defined as

$$n_{ib}^2(x) = \gamma n_{io}^2 e^{\Delta E_{gb}^{app}/kT} e^{[\Delta E_{g,Ge}(grade)]x/(W_b kT)} e^{\Delta E_{g,Ge}(0)/kT} \tag{12}$$

where

$$\Delta E_{g,Ge}(grade) = \Delta E_{g,Ge}(W_b) - \Delta E_{g,Ge}(0) \tag{13}$$

and $\Delta E_{gb}^{app}/kT$ refers to the heavy doping induced apparent bandgap narrowing in the base. The low-doping intrinsic carrier density for Si is known be

$$n_{io}^2 = N_C N_V e^{-E_{go}/kT} \tag{14}$$

and the "effective density-of-states ratio" between SiGe and Si [30] is

$$\gamma = (N_C N_V)_{SiGe}/(N_C N_V)_{Si} < 1 \tag{15}$$

Putting all these together, gives the equation for J_C in a SiGe HBT ([31]-[32])

$$J_{C,SiGe} = \frac{qD_{nb}}{N_{ab}^{-}W_b}\left(e^{qV_{BE}/kT}-1\right)n_{io}^2 e^{\Delta E_{gb}^{app}/kT}\left\{\frac{\widetilde{\gamma}\widetilde{\eta}e^{\Delta E_{g,Ge}(0)/kT}\Delta E_{g,Ge}(grade)/kT}{1-e^{-\Delta E_{g,Ge}(grade)/kT}}\right\} \quad (16)$$

where $\widetilde{\gamma}$ is position-averaged and $\tilde{\eta} = \left(\widetilde{D_{nb}}\right)_{SiGe}/(D_{nb})_{Si}$ is the minority electron diffusivity ratio between SiGe and Si. It is observable that the first term in Equation 16 refers

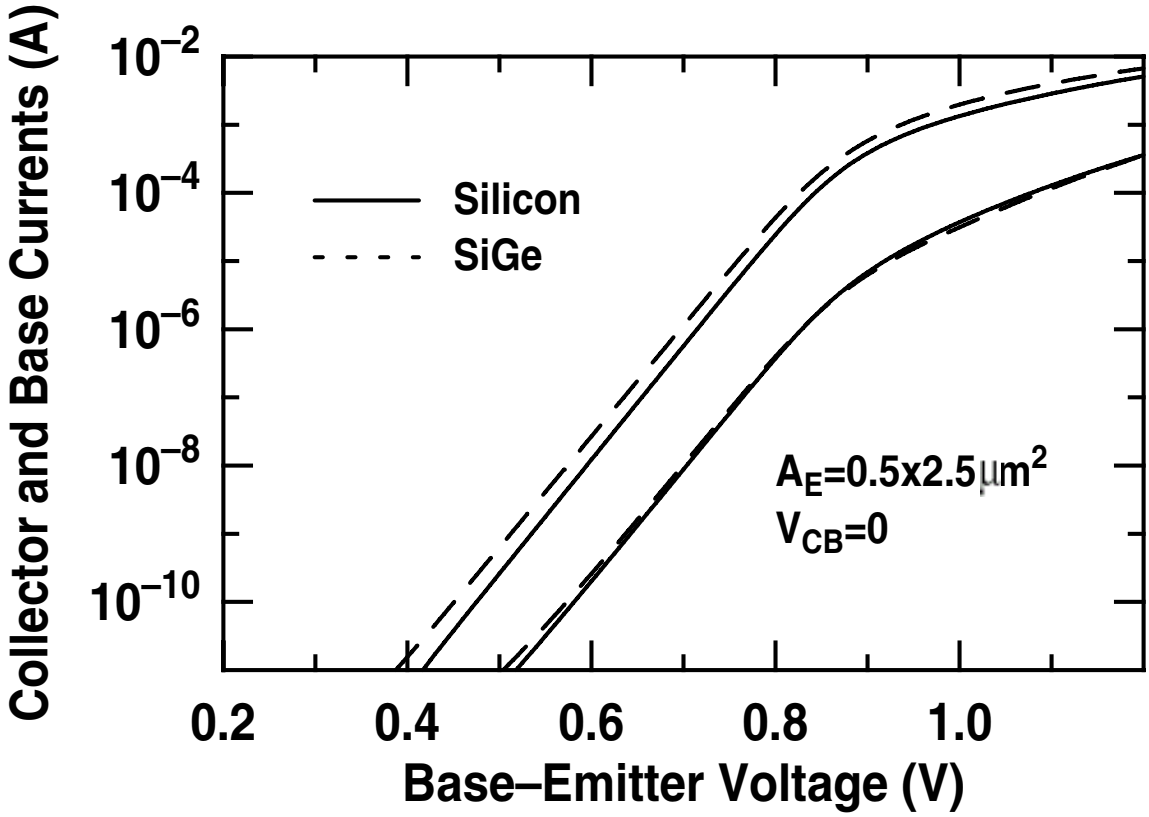

Figure 10: Representative Gummel characteristics for a SiGe HBT as compared to a Si BJT (after [16]).

to the J_C of a Si BJT and the second term corresponds to the effect of Ge content in the base. Equation 16 provides a basis for comparison between the Gummel characteristics for a typical SiGe HBT and a identically fabricated Si BJT, as shown in Figure 10. The collector current enhancement in SiGe HBT compared to Si BJT is noticeable, as discussed before in the context of bandgap reduction. Since the base current does not change much,

the current gain also increases in SiGe HBT (Equation 17).

$$\frac{\beta_{SiGe}}{\beta_{Si}} \cong \frac{J_{C,SiGe}}{J_{C,Si}} = \frac{\widetilde{\gamma}\widetilde{\eta}\Delta E_{g,Ge}(grade)/kTe^{\Delta E_{g,Ge}(0)/kT}}{1-e^{-\Delta E_{g,Ge}(grade)/kT}} \tag{17}$$

The dynamic output conductance effect of a transistor is known as Early Voltage (V_A). It essentially describes the increase of I_C due to the increase in V_{CB}. The ratio of V_A for a SiGe HBT and Si BJT is given in Equation 18, and it is an exponential function of Ge induced graded bandgap across neutral base.

$$\frac{V_{A,SiGe}}{V_{A,Si}}\Big|_{V_{BE}} = e^{\Delta E_{g,Ge}(grade)/kT}\left[\frac{1-e^{-\Delta E_{g,Ge}(grade)/kT}}{\Delta E_{g,Ge}(grade)/kT}\right] \tag{18}$$

As mentioned earlier, the shape of Ge profile has significant impact on different performance parameters. A box Ge profile is favorable for β improvement in a SiGe HBT over Si BJT, whereas triangular Ge profile is better suited for V_A enhancement. Also for analog circuits, "βV_A" product is a figure-of-merit, and is significantly enhanced in SiGe HBT over Si BJT (Equation 19). The other advantage in SiGe HBT is that both β and V_A can be adjusted independent of base profile by using different types of Ge profile shape.

$$\frac{\beta V_{A,SiGe}}{\beta V_{A,Si}} = \widetilde{\gamma}\widetilde{\eta}e^{\Delta E_{g,Ge}(0)/kT}e^{\Delta E_{g,Ge}(grade)/kT} \tag{19}$$

From a dynamic characteristics perspective, SiGe HBT has certain advantages as well. Due to the Ge-gradient-induced drift field across the neutral base in the direction from the collector to the emitter, the electrons that transit from the emitter through the base to the collector speed up. Though the bandgap offset in SiGe HBT is generally small in III-V standard measures, the electric filed that is produced is fairly large, due to the Ge-grading in the narrow base. This acceleration of electrons decreases base transit time τ_b in SiGe HBT. The comparison with Si BJT is given as follows

$$\frac{\tau_{b,SiGe}}{\tau_{b,Si}} = \frac{2}{\widetilde{\eta}}\frac{kT}{\Delta E_{g,Ge}(grade)}\left\{1-\frac{kT}{\Delta E_{g,Ge}(grade)}\left[1-e^{-\Delta E_{g,Ge}(grade)/kT}\right]\right\} \tag{20}$$

Also the forward bias in EB junction creates a back-injection of holes from the base to emitter, and gives rise to emitter charge storage delay time (τ_e), which is inversely proportional to the ac current gain β_{ac}. As seen in Equation 21, τ_e is reduced for the SiGe HBT

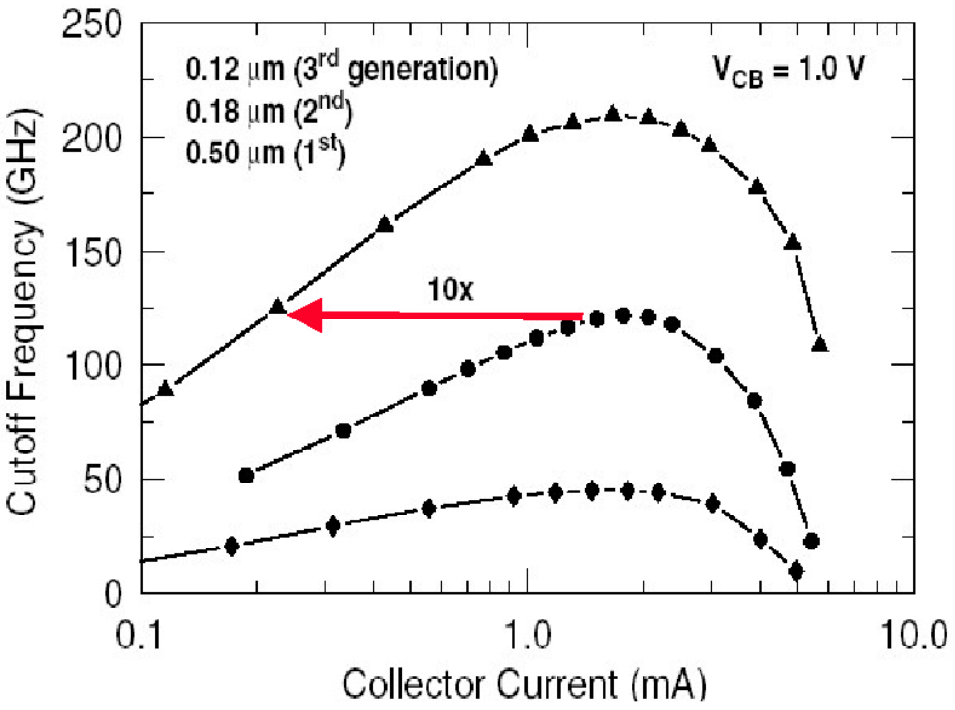

Figure 11: Cutoff frequency as a function of collector current density for three generations of SiGe HBT BiCMOS technology.

and is a stronger function of EB edge value of Ge-induced band offset, whereas τ_b depends more on the Ge grading across the base.

$$\frac{\tau_{e,SiGe}}{\tau_{e,Si}} \simeq \frac{J_{C,Si}}{J_{C,SiGe}} = \frac{1 - e^{-\Delta E_{g,Ge}(grade)/kT}}{\widetilde{\gamma}\widetilde{\eta}\frac{\Delta E_{g,Ge}(grade)}{kT} e^{\Delta E_{g,Ge}(0)/kT}} \tag{21}$$

The unity-gain cutoff frequency f_T in a BJT is is given by:

$$f_T = \frac{1}{2\pi}\left[\frac{1}{g_m}(C_{eb} + C_{cb}) + \tau_b + \tau_e + \frac{W_{CB}}{2v_{sat}} + r_c C_{cb}\right]^{-1} \tag{22}$$

where $g_m = \frac{kT}{qI_C}$ is the low-injection intrinsic transconductance, C_{eb} and C_{cb} are the EB and CB depletion capacitances, W_{CB} is the CB space-charge region width, v_{sat} is the saturation velocity, and r_c is the collector resistance (dynamic). As seen earlier, τ_b and τ_e decreases in SiGe HBT, and therefore, increases f_T. Figure 11 shows f_T vs. I_C for three generations of SiGe HBT devices.

The maximum oscillation frequency f_{max} is defined as:

$$f_{max} = \sqrt{\frac{f_T}{8\pi C_{cb} r_b}} \tag{23}$$

where r_b is the *ac* base resistance and C_{cb} is the CB capacitance. The f_{max} of the SiGe HBT increases as f_T gets improved and r_b is reduced.

Whether f_T or f_{max} is a better figure-of-merit (FOM) for speed or bandwidth determination, depends on the specific application. In practice for SiGe devices, designs are geared more towards similar values of f_T and f_{max}.

2.5 Summary

The basic discussion on fundamental Si BJT and SiGe HBT device physics, carrier transport mechanism, different performance parameters and comparison has been presented in this chapter. For a comparably structured SiGe HBT, increased J_C, β, V_A, f_T, and f_{max} is observed over the Si BJT. SiGe HBT has other advantages like improved broadband, 1/f and phase noise performance. This chapter explains the background concepts of Si BJT and SiGe HBT, which can be applied for further investigation in different aspects, strain effects for instance in this work.

CHAPTER III

STRAIN ENGINEERING

3.1 Introduction

Strain engineering, is the application of strain on standard transistors to enhance performance without downsizing transistor dimensions. In search for alternatives to transistor scaling and new materials for improved device and circuits performance, strain engineering has become a strong contender. It has been investigated by several research groups, and has already made its place in commercial production [10]-[11]. This chapter gives an overview of different types, orientations and application techniques of strain, and the physics behind, as well as the current state of research on strain.

3.2 Types and Orientations of Strain

Strain can be of two types, tensile strain or compressive strain. Tensile strain stretches certain planes of the cubic crystal structure of Si, while compressive strain, as the name suggests, compresses Si. Industry standard Si wafers are oriented in (001) surface, with the wafer notch on [110] direction [33]-[34] . The channel of the MOSFET(NMOSFET/PMOSFET) transistors lay in parallel or perpendicular to the [110] direction. The applied strain, thus may be along, parallel or perpendicular to the channel. Depending on the direction of strain application, strain effects are discussed under two categories, namely biaxial strain and uniaxial strain. Biaxial strain is applied in the channel plane, which has components in the direction (or parallel) of the channel as well as in perpendicular to the channel. These directions are often termed as longitudinal and transverse directions [33] or X and Y directions [35]. Unlike biaxial strain, uniaxial strain is applied in a certain direction.

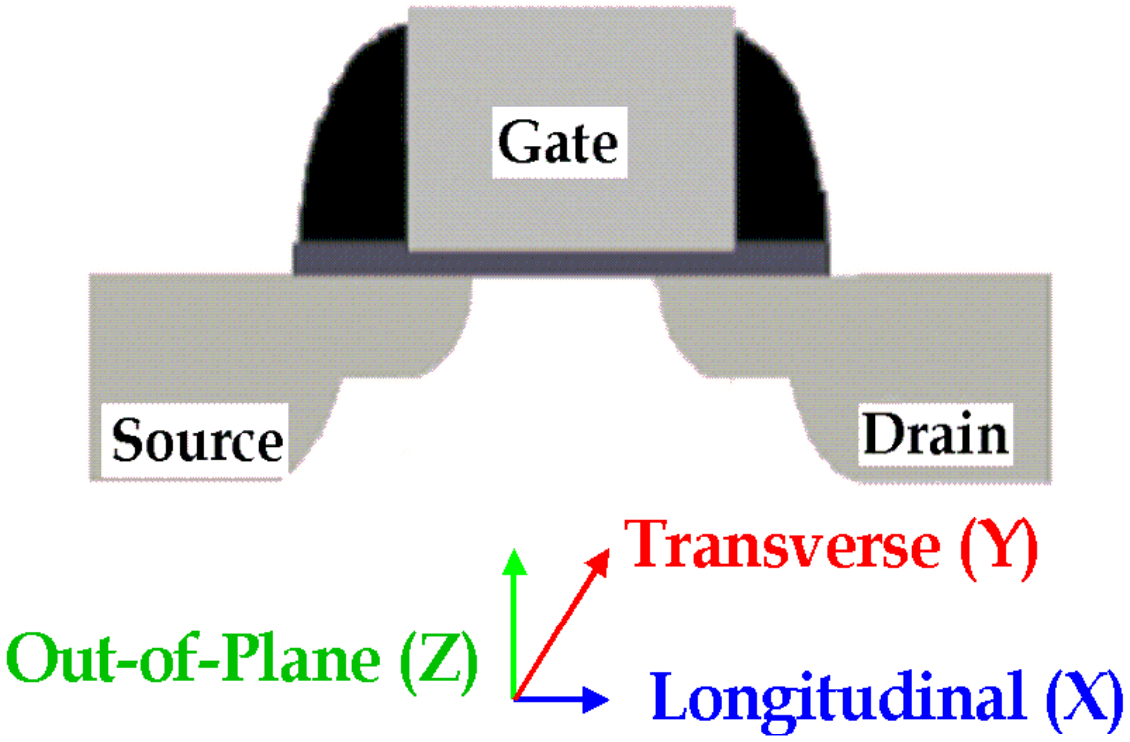

Figure 12: Definition of strain direction in MOS devices (after [33]).

Table 1: Required stress types for enhanced mobility.

Direction of Strain	**NMOS**	**PMOS**
Longitudinal (X)	Tensile	Compressive
Transverse (Y)	Tensile	Tensile
Out-of-plane (Z)	Compressive	Tensile

Depending on the direction applied, uniaxial strain can have drastically different implication [34]-[36]. Strain can also be in the Z or out-plane direction. Therefore, strain can be applied in one, two or even in three dimensions as well. Strain directions, from a MOS transistor perspective are shown in Figure 12. The direction and type of strain determines the performance improvement of transistors due to strain. This improvement, is however a function of transistor types as well, that is NMOS and PMOS devices are affected differently under different types and orientations of strain. Table 1 summarizes the required types of strain for each type of transistors [33]. It is observable that, tensile strain in the

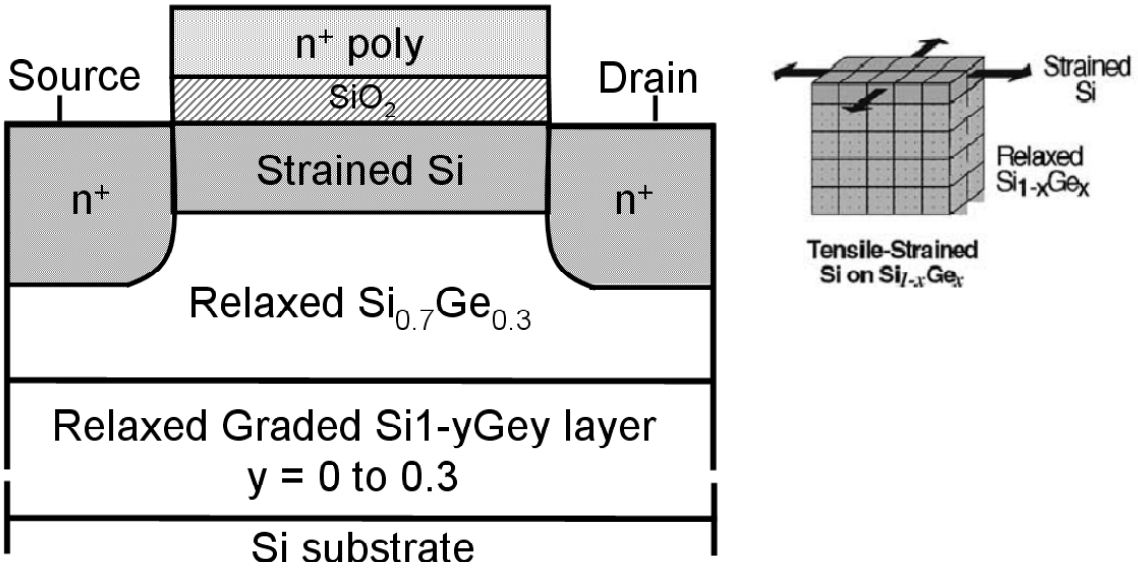

Figure 13: Strained Si/relaxed $Si_{1-x}Ge_x$ NMOSFET and biaxial tensile strain (after [12],[37]).

transverse direction positively affects both NMOS and PMOS devices. Another key point is that, NMOS transistors work better under tensile strain, while compressive strain improves PMOS performance.

3.3 Strain Application Techniques

The engineering of strain has been mostly on CMOS process. Therefore, the techniques of applying strain are often CMOS process specific. The application of strain in the channel of a MOSFET transistor has been approached in mostly two ways, often termed as Global Strain and Local Strain [10],[12]. A third way of strain application is Mechanical Strain. In SiGe HBTs, introduction of Ge in the narrow base introduces strain, which can be viewed as local in nature. However, from a strain effect investigation perspective, bipolar and heterojunction bipolar devices have been strained in a mechanical manner only.

3.3.1 Global Strain

In this method, strain is applied at the wafer level. There has been different approaches to achieve this. Most common method is to grow a thin layer of strained Si on top of a crystalline lattice with a larger lattice constant than Si [40]-[49]. This lattice is typically relaxed $Si_{1-x}Ge_x$ grown on Si wafers, as depicted in Figure 13. This method, known as the Si-SiGe lattice mismatch method, induces biaxial tensile strain on the Si channel. This is due to the fact that, the top Si layer expands along the XY plane to match the larger (about 4.2%) lattice constant SiGe underneath. As the percentage of the Ge gradually increases in the SiGe layer, the strain on the Si channel is enhanced. About 2x improvement in the electron and hole mobility for nMOS (upto larger vertical electric field E_{eff}) and pMOS (for low E_{eff}) has been reported for strained Si on relaxed SiGe [12].

The advantage of global strain is that, it is wafer-level and the transistor fabrication process requires little or no change. However, there are several process integration issues due to the presence of Ge, like Ge up-diffusion, relaxation of SiGe via misfit dislocation formation and thermal processing during the CMOS fabrication steps [38]. Off leakage current (I_{OFF}) via misfit dislocation and lower threshold voltage (V_T) [12],[37],[50], and larger overlap capacitance are some of the other issues. From a cost perspective, SiGe layer is generally quite thick, which is formed after longer period of expensive deposition. It is worth mentioning that NMOSFET enhancements saturate at around 20% Ge content, but PMOSFET hole mobility shows superior performance upto 40% Ge [39]. As a matter of fact, for PMOS enhancement via hole mobility improvement, a larger amount of strain is required (higher Ge content), which has practical challenges and issues associated with it [37]. Another problem is that the PMOS enhancement is mostly at low electric fields (< 1 MV/cm), and the improvement diminishes at large vertical electric fields [43]. In spite of all these disadvantages, global method of strain serves as a basis for fundamental understanding of strain engineering. Also it is highly suited for Silicon-on-Insulator (SOI) technology [10],[12].

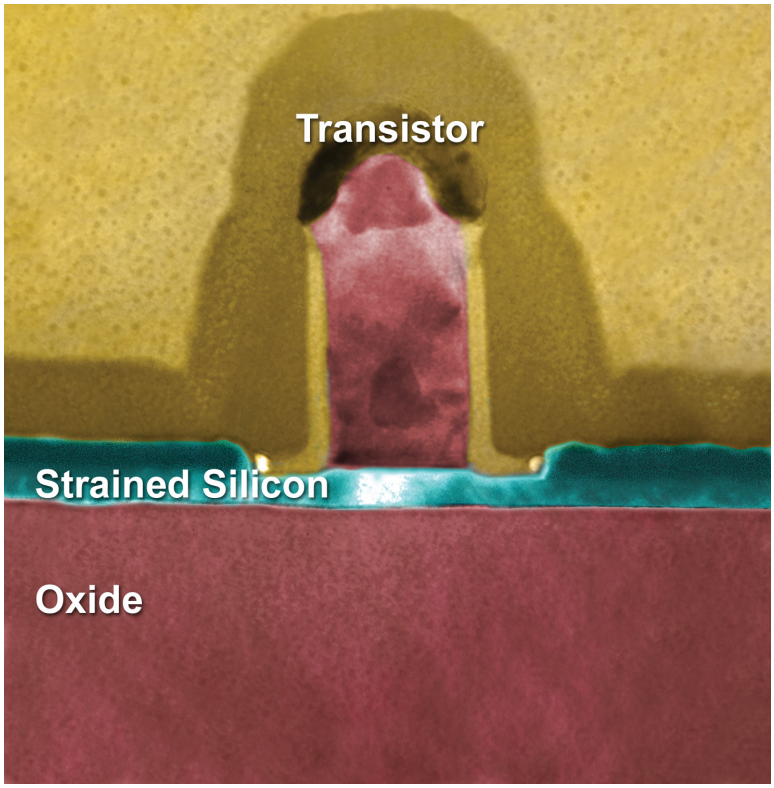

Figure 14: Fabricated SSDOI or Strained Si transistor Directly on Insulator (after [51]).

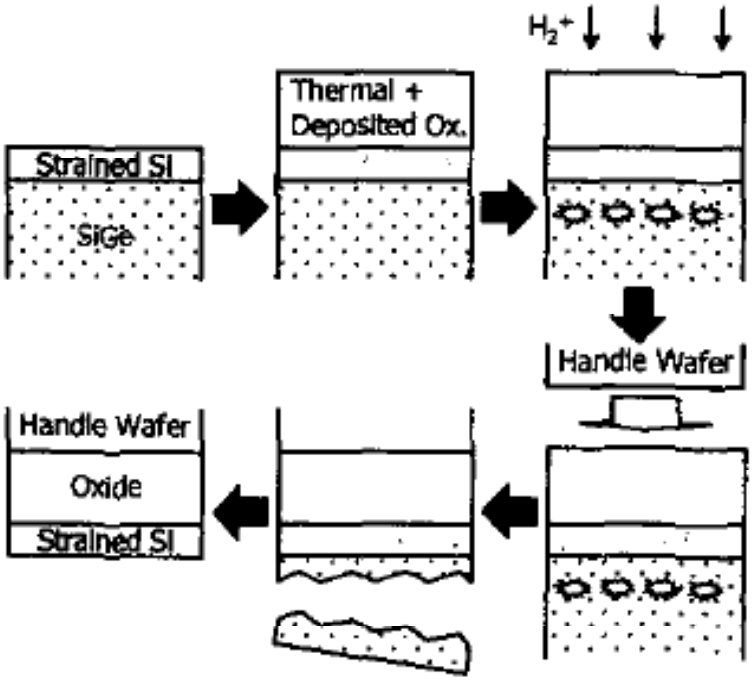

Figure 15: Process flow for SSDOI (after [52]).

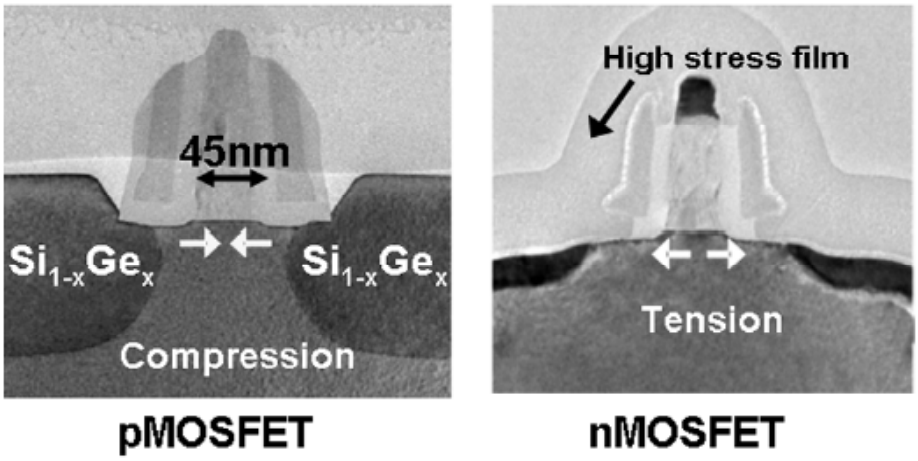

Figure 16: TEM micrographs of 45 nm PMOSFET and NMOSFET, from 90 nm technology (after [36]).

IBM, AmberWave Systems and other companies have used global strain using relaxed SiGe, as well as using another technique called Strained Si Directly on Insulator (SSDOI) or Strained Si on Insulator (SSOI) (Figure 14). SSDOI or SSOI overcomes some of the disadvantages like Ge-diffusion and stringent thermal budget constraints of global strain applied via strained Si on relaxed SiGe. In this technique, strained Si layer grown on relaxed SiGe is transferred to an an oxidized Si wafer, after removal of the SiGe [52]-[53]. The process flow for SSDOI is shown in Figure 15.

3.3.2 Local Strain

Local strain refers to different process-induced strains, either uniaxial or biaxial, to optimize NMOSFET and PMOSFET devices on the same wafer independently by applying different levels of strain [36]. The challenge in this technique is to develop high stress inducing films that are compatible with current production, for higher integration. Nitride and oxide are two common local strain inducer. Recently Intel has implemented process induced strain in their 90 nm technology and beyond, where SiN (Silicon Nitride) cap layer has been used to apply tensile strain through gate stack for NMOFETS.

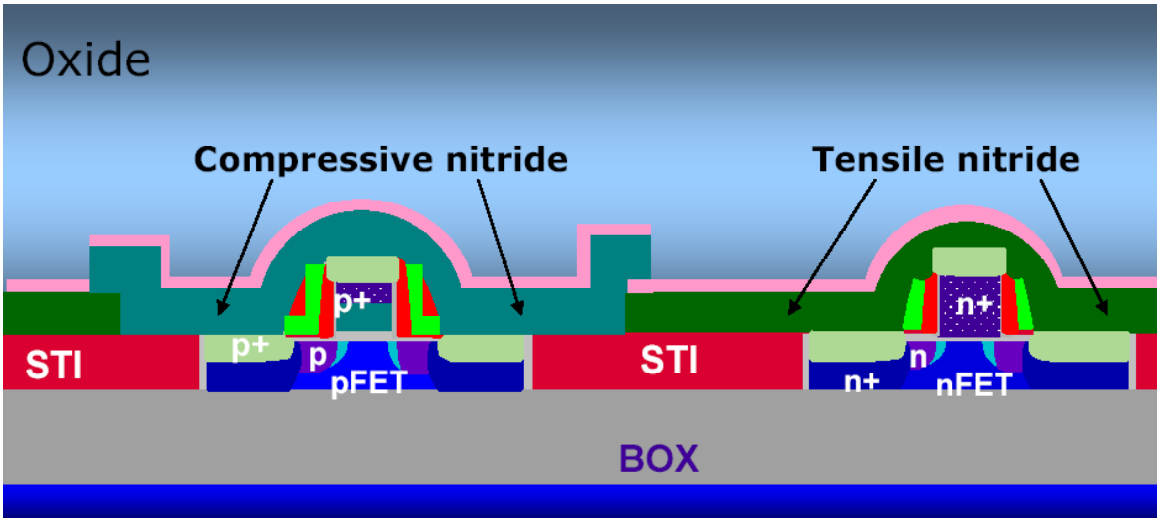

Figure 17: Local strain using dual stress liner for 45 nm CMOS (after [57]).

For the PMOSFETs, the drain and source regions are substituted by SiGe, which generates compressive uniaxial strain in the channel, and increases hole mobility. This, however has the risk of Ge diffusion in the channel. Figure 16 illustrate the implementation of process induced strain by Intel. Another process, known as 'dual stress liners' (Figure 17), uses tensile nitride cap layers for NMOS, and compressive nitride overlayer for PMOS. This method has been adapted by Advanced Micro Devices (AMD) and International Business Machines (IBM) [57]-[58], for their sub-45 nm gate length CMOS. The other type of stress inducing films are oxides that are used in shallow-trench isolation (STI) and premetal dielectric (PMD) fill. Though process induced local strain can be very effective, it comes at the cost of more complex processing steps. Also in process induced straining method, any small variation can have quite significant impact as strain is applied locally on certain areas. However, rigorous manufacturing control can overcome these shortcomings.

3.3.3 Mechanically Induced Strain

Mechanically induced strain is applied post fabrication, unlike the two other techniques mentioned above [13]-[15], [34],[59]-[66]. This is often done by mechanically bending the wafer [14],[63]-[65], as shown in Figure 18 and Figure 19. Within mechanical paradigm,

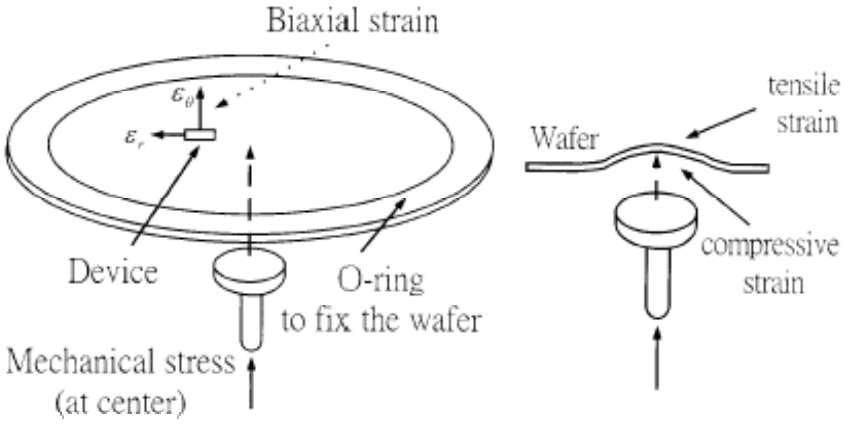

Figure 18: Strain application by external mechanical bending (after [14]).

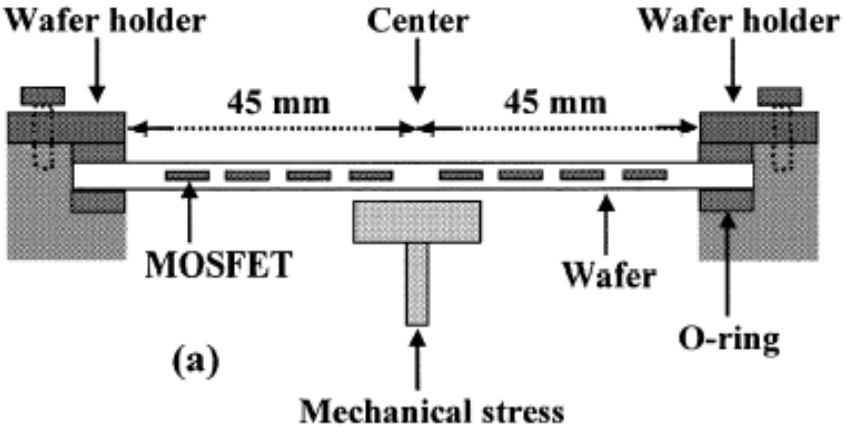

Figure 19: External application of strain by mechanical bending (after [65]).

Belford Research Inc. has implemented strained devices using a unique process [13], [34], [59]-[60]. In this method, the device layer is separated from the bulk layer, and then the device layer is affixed to a planar or bent substrate [61]-[62]. This process is a back-end process [59]. This is explained in more detail in Chapter IV. This thesis uses samples prepared in such manner, by Belford Research Inc. The biggest advantage of mechanical strain is that no change in the process flow of transistor fabrication is required, which in turn assures lower cost as it is very expensive to modify the process technology. The disadvantage of mechanical strain can be reliability concern, which needs to be further analyzed.

3.4 Physics of Strain

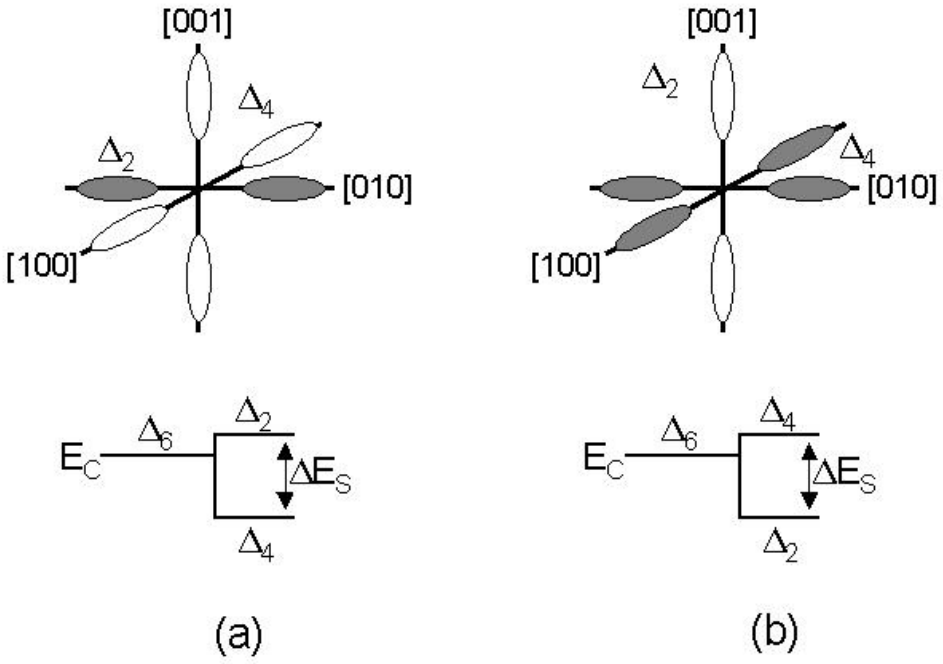

Figure 20: Conduction band splitting for (a) uniaxial strain and (b) biaxial strain.

Biaxial strain breaks the physical and electrical symmetry of both the conduction and valence bands of unstrained Si. Uniaxial strain, in general, also changes both the bands of Si. The differences between the conduction band splitting for uniaxial and biaxial strain is

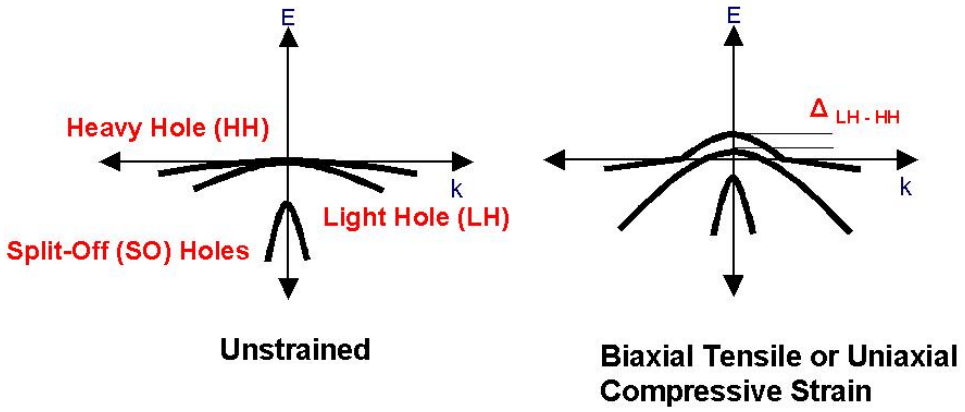

Figure 21: Valance band splitting comparison for unstrained and strained Si (after [33]).

illustrated in Figure 20.

For biaxial strain, the previously degenerate 6-fold Si conduction band is splitted [40]-[49]. The energies of the two perpendicular or out-of-plane valleys (Δ_2) are lowered in comparison to the four in-plane valleys (Δ_4). For biaxial strain induced using Si on relaxed $Si_{1-x}Ge_x$, the conduction band energy splitting between two out-of-plane minima on [001] axes and four in plane minima on [100] and [010] axes is about ΔE_S = x0.67 eV or ΔE_S = 67 meV/10%Ge [37],[40]-[43]. After strain, the variation in the effective mass of electrons in a particular conduction band valley is negligible, compared to the unstrained Si. In an individual conduction band valley, the electrons retain their longitudinal (along the valley) and transverse (perpendicular to the valley) effective masses to be about $0.19m_o$ and $0.91m_o$ respectively [40]. However, due to the redistribution of electrons across different conduction band valleys, the net in-plane effective mass goes down. This redistribution occurs as electrons tend to inhabit the lowest energy state, and more electrons preferably occupy the out-of-plane lower energy Δ_2 valleys for biaxial strain. The in-plane effective mass in the Δ_2 valleys is lower ($m^* = 0.19m_o$), and thus overall in-plane effective mass decreases. This results in higher electron mobility in the direction of electron flow at low effective electric field (E_{eff}). The other reason of increased electron mobility is the suppression of inter-valley phonon-carrier scattering between the Δ_2 and Δ_4 valleys, due to their difference in

energy levels [44],[46]. Therefore, very often in literature, the reduction of total in-plane effective mass and inter-valley scattering due to strain are quoted as the reasons for electron mobility or NMOSFET performance enhancement [45],[47].

The biaxial tensile strain induced by Si-SiGe lattice mismatch method also creates a split in the valence band degeneracy (40 meV/10% Ge content) [43], like the conduction band. In the valence band, biaxial strain reduces the heavy hole and split off band energies with respect to the light hole band [44], as shown in Figure 21. It is instructive to observe that, the subband splitting of valence band is lower than in the conduction band, thus explains the higher level of strain requirement for PMOSFET performance enhancement.

The applied strain alters the shape of valence subbands, while leaving the shape of the conduction bands unchanged [40]-[44].

Uniaxial strain also modifies both the conduction and valence bands of Si. The applied strain breaks the sixfold degeneracy of the Si conduction band. However, in contrary to the biaxial strain, the energies of the four perpendicular or normal valleys (Δ_4) are reduced with respect to the two longitudinal valleys (Δ_2), along which strain is applied.

3.5 Summary

In order to extract maximum benefit out of standard BJT/HBT by applying strain, a thorough knowledge and understanding of strain physics is required. Strain can be applied in different ways, and every technique has its benefits and problems over the other methods. This chapter has covered an overview of strain engineering and the current state of strain application.

CHAPTER IV

STRAIN EFFECTS IN BJT/HBT DEVICES

4.1 Introduction

Strain effects in BJT/HBT has not been explored in great detail. This thesis is focused on the study of strain induced effects on these devices. In this work, first order effects are treated with great importance, as this will lay down the background for further analysis. Both biaxial and uniaxial strain has been explored for SiGe devices. Si BJTs were examined under biaxial strain only. Biaxially strained devices were characterized for static (*dc*) and dynamic (*ac* or high frequency) analysis, whereas uniaxially strained samples were investigated under static conditions only.

4.2 Device Technology

In this experiment, both biaxial and uniaxial strain effects on Si BJT/SiGe HBT has been researched. For biaxial strain, three fully-integrated self-aligned BiCMOS technologies from two distinct generations of devices from IBM were investigated in this study. The first generation SiGe HBT BiCMOS technology (IBM 5HP) incorporates 0.50μm, 3.3 V

Table 2: Device technology for Si/SiGe BiCMOS technologies (after [16]).

Si/SiGe BiCMOS Technology Parameters	IBM 5HP Si BJT/SiGe HBT	IBM 7HP High Performance	IBM 7HP High Breakdown
Drawn Emitter Width (μm)	0.5	0.2	0.2
Actual Emitter Width (μm)	0.42	0.18	0.18
V_A (V)	65	120	120
BV_{CEO} (V)	3.3	1.8	4.3
Peak f_T (GHz)	50	120	35
Peak β	113	543	543

BV_{CEO}, 50GHz peak f_T SiGe HBTs with the 0.35μm standard Si CMOS [67]. For this generation, Si BJTs have a 0.50μm epitaxial base Si BJT control (fabricated identically in the same wafer lot as the SiGe HBT) with 0.35μm standard Si CMOS (identical to the Si CMOS on the SiGe HBT wafer). The second generation SiGe HBT BiCMOS technology (IBM 7HP) combines 0.18 μm, 1.8 V BV_{CEO}, 120 GHz f_T SiGe HBTs ("High Performance") and 4.3 V BV_{CEO}, 35 GHz f_T SiGe HBTs ("High Breakdown"), with three distinct versions of 0.18μm Si CMOS devices [28]. Table 2 summarizes different device parameters for Si BJT/ SiGe HBTs across two different technology generations from IBM. For the uniaxial strain study, the second generation of SiGe HBTs mentioned above have been used.

4.3 Strain Sample Preparation

Initially the wafers were diced and thinned to flexible membrane dimensions (25-30 μm thickness). Planar biaxial strain was achieved by using a novel differential thermal bonding technique [61]–[62], in which the thinned membrane was bonded to a substrate of different coefficient of thermal expansion (CTE) at high temperature. The biaxial strain is induced as the bonded pair returns to ambient temperature (see Figure 22). The applied biaxial tensile strain was calculated to be 0.123% for the *dc* samples. The amount of strain for the SiGe HBT *ac* sample was about 0.057%, with a biaxial component of 0.035% and a uniaxial component of 0.022%. For the Si BJT *ac* sample, a biaxial component of 0.035% and a uniaxial component of 0.010% makes a total strain of 0.045%. These samples were strained using the differential thermal bonding technique as well[62].

For the uniaxial samples, The thin device membrane was affixed to the surface of a curved or cylindrical substrate. The physical stretching resulting from the bonding induces a controlled value of uniaxial tensile strain in the sample [61]. The applied uniaxial tensile strain for the second-generation devices was calculated to be 0.066%. The structure of the uniaxially strained sample is shown in Figure 23.

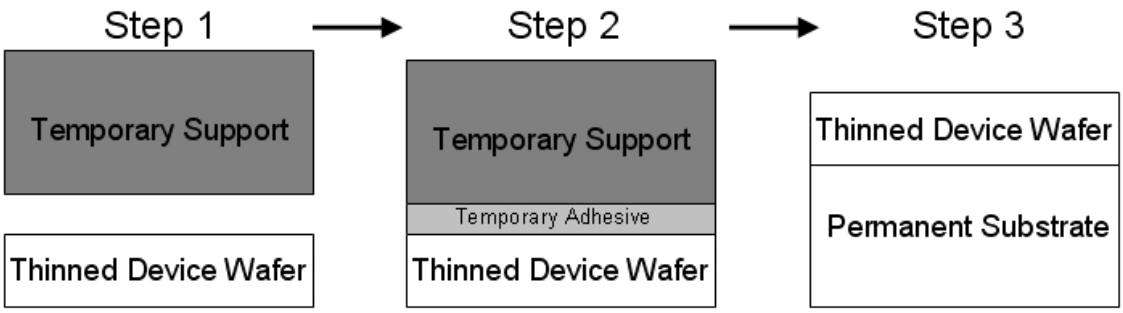

Figure 22: Process flow for the planar biaxial strain by differential thermal bonding.

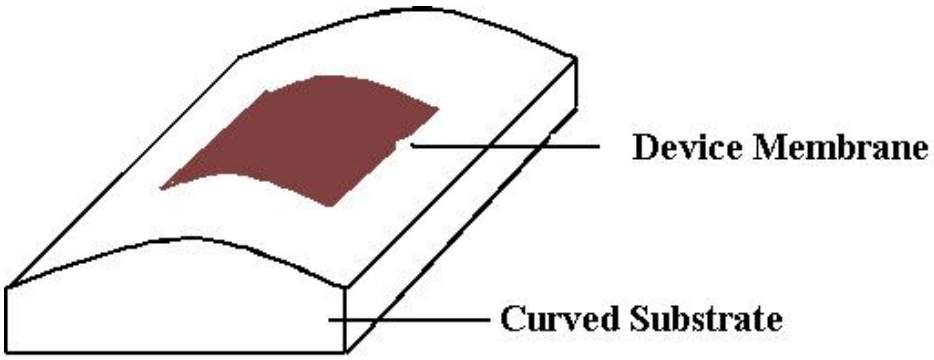

Figure 23: Mechanically-induced strained uniaxial samples.

4.4 Experimental Setup

On-wafer room temperature measurements were performed using an Agilent 4155 Semiconductor Parameter Analyzer (for *dc*) and an Agilent 8510C Vector Network Analyzer (for *ac*) on a temperature-controlled probe station (manufactured by Wentworth). KNS automatic probe cards were used for probing the devices on the wafer. In general, gummel (I_C,I_B vs. V_{BE}) and output (I_C vs. V_{CE}) measurements were performed for *dc* characterization. After the pre-strain measurements were performed the wafers were diced. Then using the novel differential thermal bonding technique, the dies were strained. These strained samples were then carefully re-characterized post-strain under identical conditions.

4.5 *Biaxial Strain Results*

Biaxially strained samples were examined for changes in both static and dynamic characteristics that may be induced by applied mechanical strain.

4.5.1 Static Characteristics

The static or *dc* characteristics study of biaxially strained devices is focused on the modifications observed in collector current, base current and current gain due to the strain. The

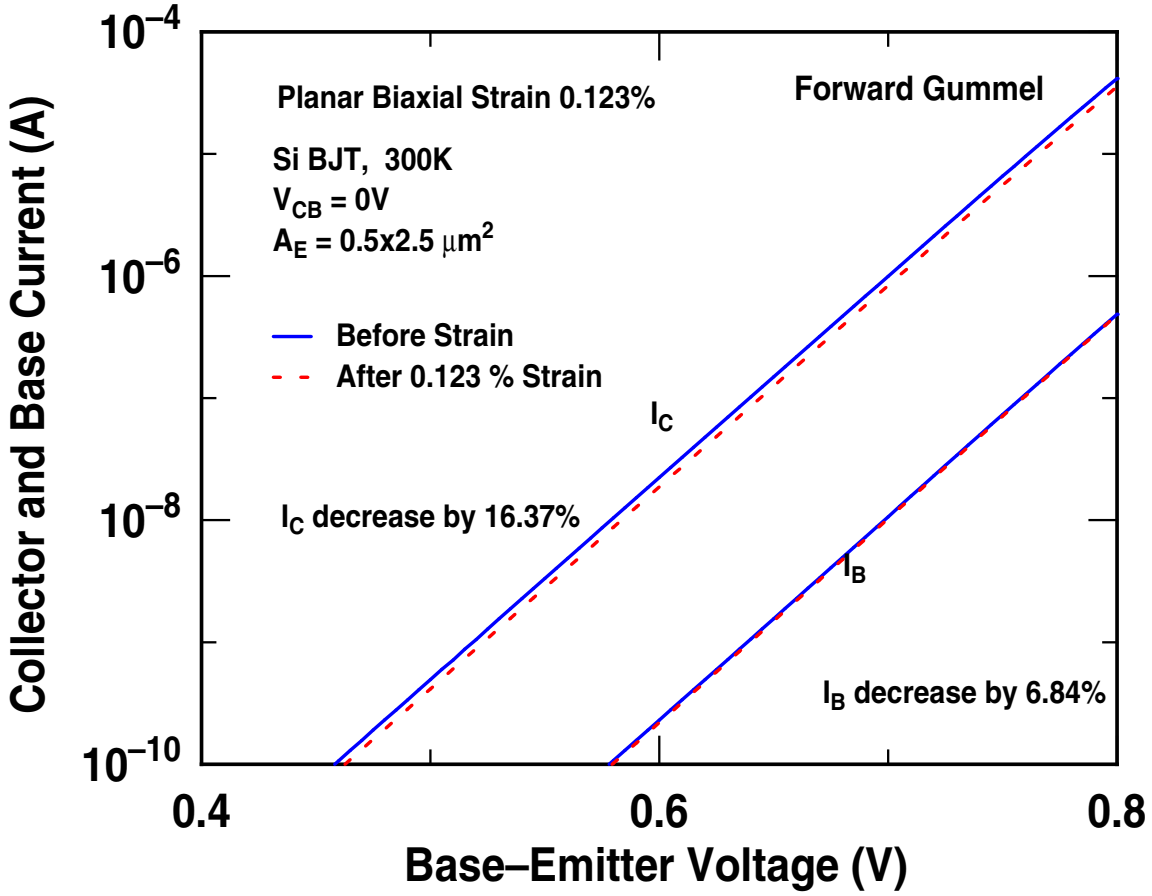

Figure 24: Forward Gummel characteristics of a Si BJT for both pre-strain and post 0.123% biaxial strain.

pre- and post-strain forward Gummel characteristics for the 5HP (0.50μm emitter width) Si BJT are shown in Figure 24. The emitter area for this particular device was 0.5x2.5μm^2. The Gummel characteristics in these membrane-thickness samples remain ideal to low

leakage levels (upto pA levels), indicating the robustness of the devices to induced defects from this straining technique. After strain, the Si BJTs exhibit up to 16.37% decrease in collector current (I_C) and 6.84% decrease in base current (I_B) at $V_{BE} = 0.7$V. The decreasing trend of both I_C and I_B was statistically persistent for three other same geometry (emitter area) Si BJT devices. In addition to forward mode Gummel characteristics, inverse mode Gummel measurements were performed. The degradation in I_C and I_B showed up in inverse mode Gummel characteristics as well. A representative inverse Gummel plot for 5HP Si BJT is shown in Figure 25.

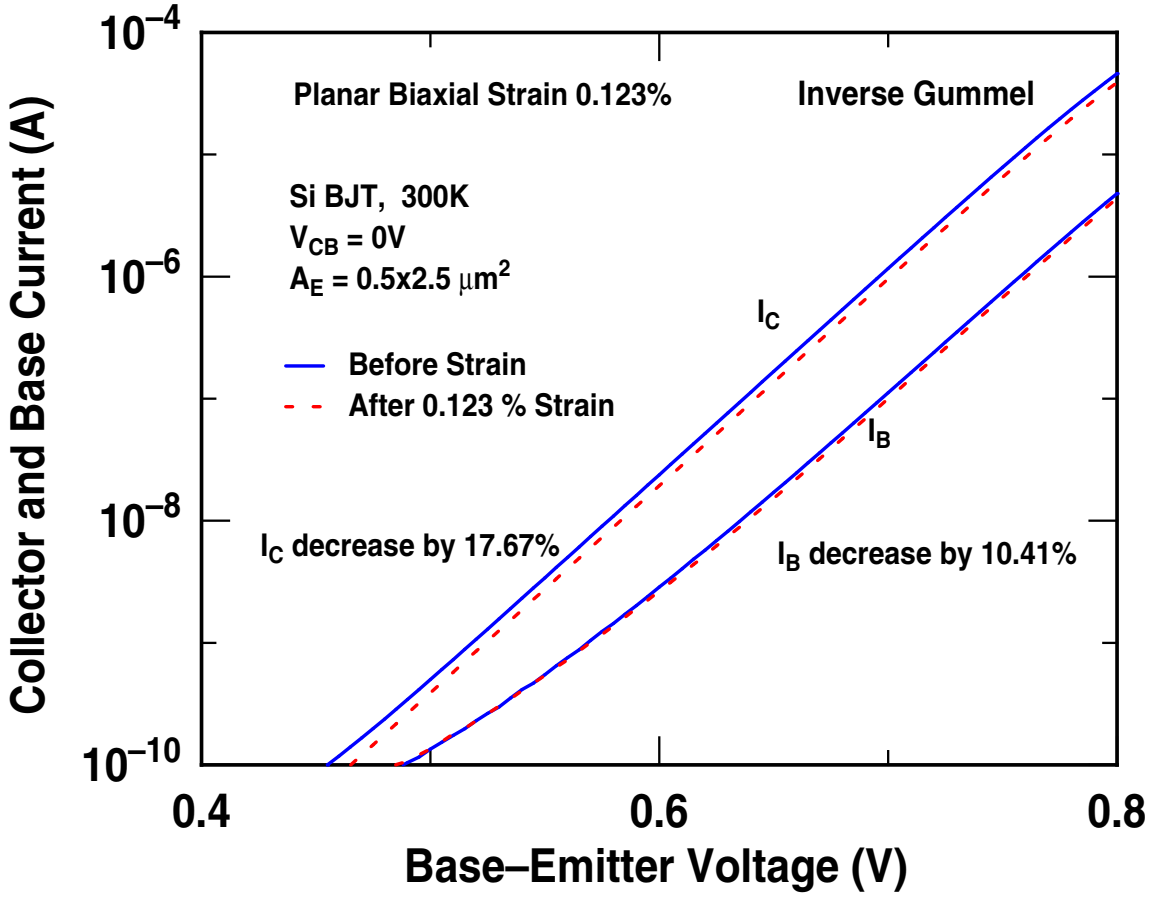

Figure 25: Inverse Gummel characteristics of a Si BJT for both pre-strain and post 0.123% biaxial strain.

For the 5HP (0.50μm emitter width) SiGe HBTs (also of emitter area 0.5x2.5μm^2), up to 9.12% decrease in I_C and up to 5.13% increase in I_B are observed (Figure 26) at the

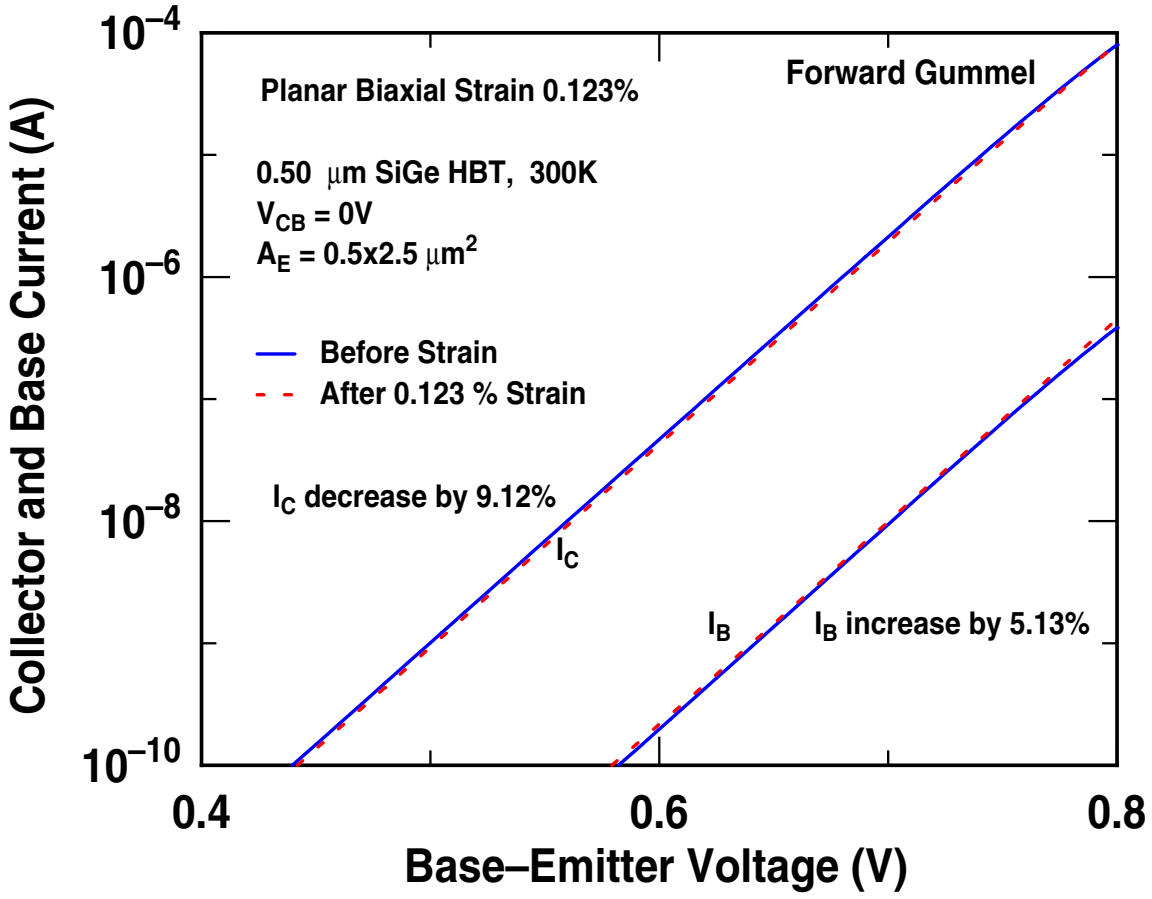

Figure 26: Forward Gummel characteristics of a first-generation SiGe HBT for both pre-strain and post 0.123% biaxial strain.

same V_{BE} after strain. The higher current gain in the SiGe HBTs compared to identical Si BJT (same transistor geometry and technology) is noticeable from the larger gap between I_C and I_B in Figure 26 than in Figure 24, which nicely coincides with theory and earlier experimental results. The higher current or injection region of both 5HP Si BJT and SiGe HBT start at around $V_{BE} = 0.9$ V, where the collector and base currents begin to fall off. The 7HP (0.18μm emitter width and 120GHz) SiGe HBTs demonstrate changes similar to the 5HP 0.50μm SiGe HBTs, a decrease in I_C and increase in I_B at 300K after strain. Figure 27 indicates that at $V_{BE} = 0.7$V, the collector current decreases by 2.05% and base current increases by 5.76% for the high performance SiGe HBT device of 0.2x19.2μm^2 emitter area. Other transistor geometries of this technology also show similar behaviour.

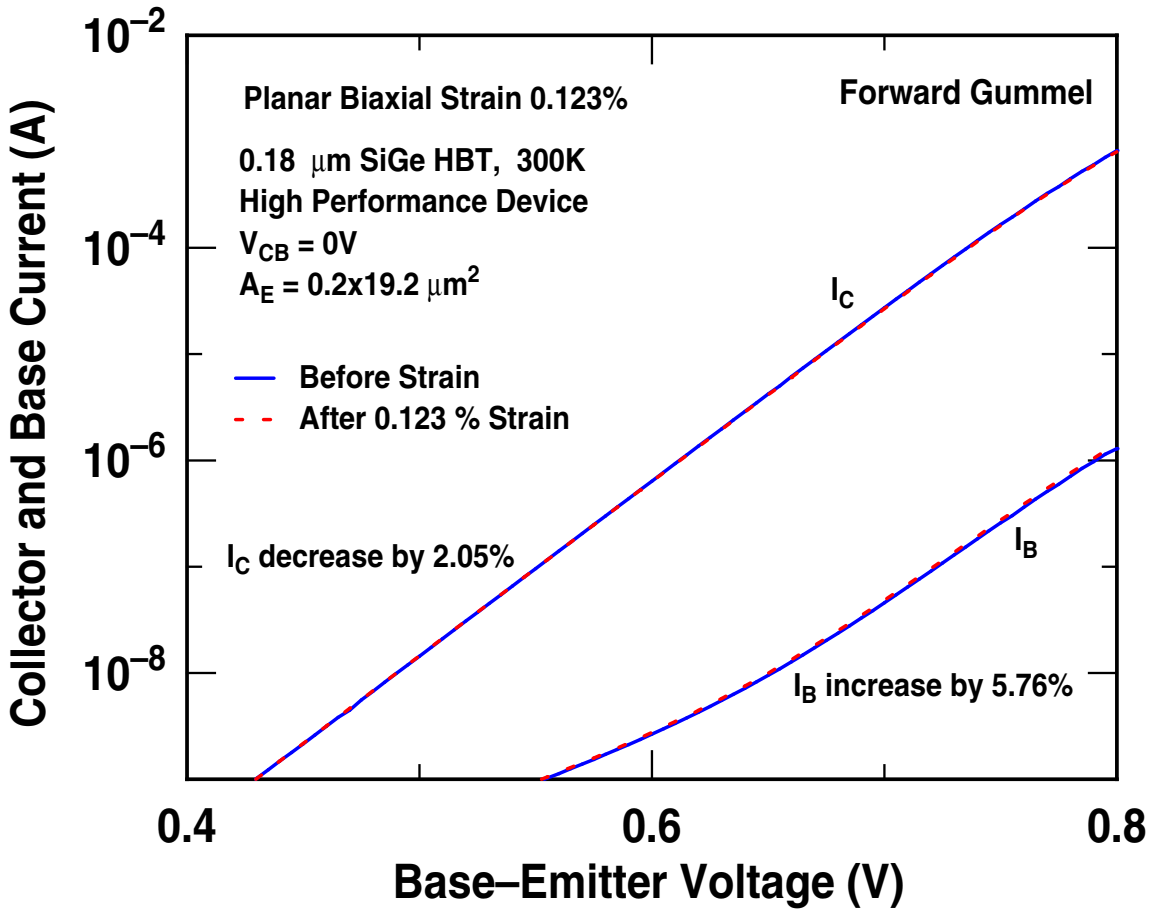

Figure 27: Forward Gummel characteristics of a second-generation high performance SiGe HBT for both pre-strain and post 0.123% biaxial strain.

The Gummel plot (Figure 26) for the 5HP SiGe HBT displays only the ideal region of I_C and I_B at moderate current levels and constant current gain (β). However, the 7HP Gummel plot (Figure 27) also exhibits the low current level region, where additional component of I_B accounts for decrease in β. This base current component, I_{B2} is due to the recombination of minority carrier electrons in the base, as explained in chapter II.

The reduction in the collector current after strain can also be seen in the forced I_B output characteristics (I_C vs. V_{CE}) of the devices. The output characteristics for the 5HP Si BJT are displayed in Figure 28, which demonstrates a 12.35% decrease in I_C at I_B = 300nA and V_{CE} = 1.5 V. For the 5HP (0.50μm) SiGe HBTs, about 12.42% decrease in I_C is observed for similar I_B and V_{CE} (Figure 29). The 7HP (0.18μm) SiGe HBTs

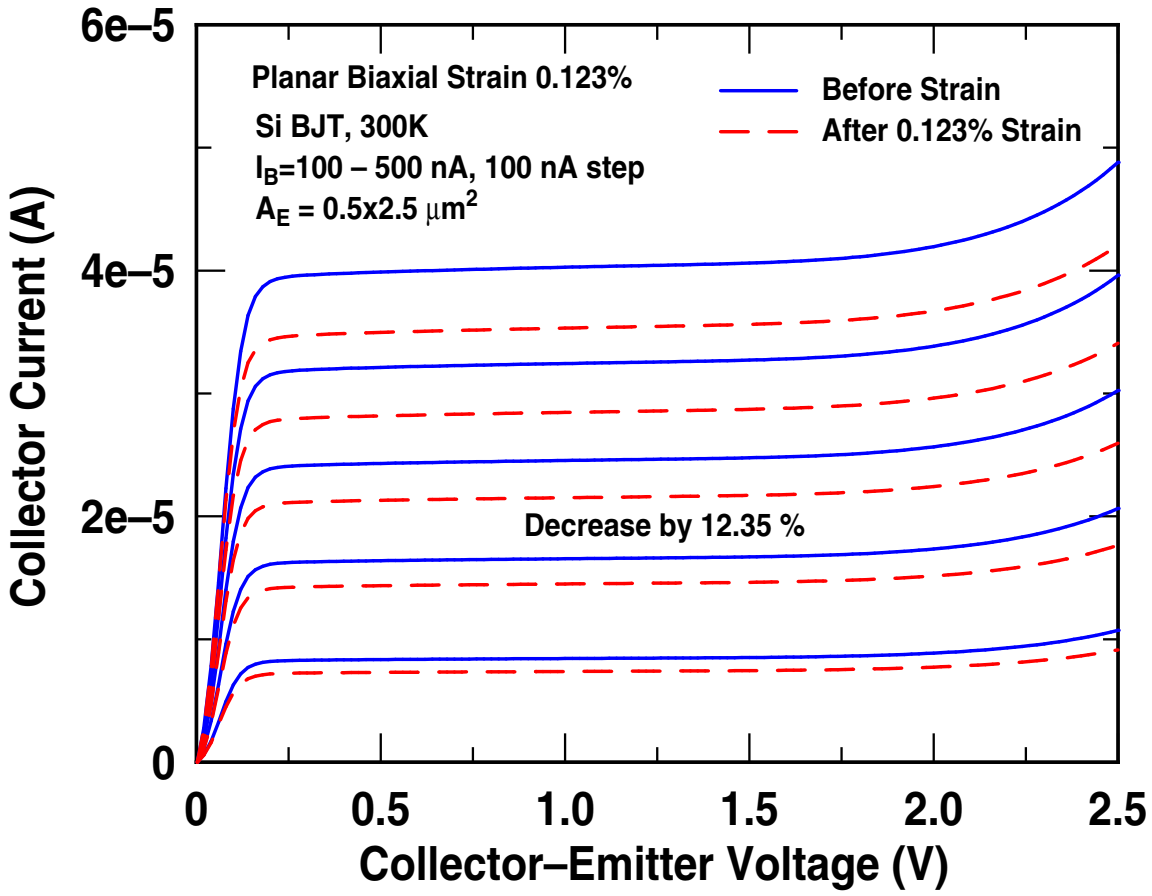

Figure 28: Output characteristics of a Si BJT for both pre-strain and post 0.123% biaxial strain.

show (Figure 30) 6.57% reduction in I_C for I_B = 45.15 μA and same V_{CE}. All the output characteristics plots show no

The output characteristics for both 5HP Si BJT and 5HP SiGe HBT was captured at the ideal region where current gain (Figure 31) variation is negligible . The maximum I_B forced was 500 nA, which corresponds to V_{BE} = 0.8 V and I_C smaller than 0.1 mA. It is observed that the roll-off of current gain (β) occurs at I_C larger than 0.1 mA, which confirms the ideal region operation of the output curves. For the 7HP device though, the output characteristics measurements were performed at high currents region or high injection level.

Due to the decrease in collector current, both the Si BJT and the two different SiGe HBT

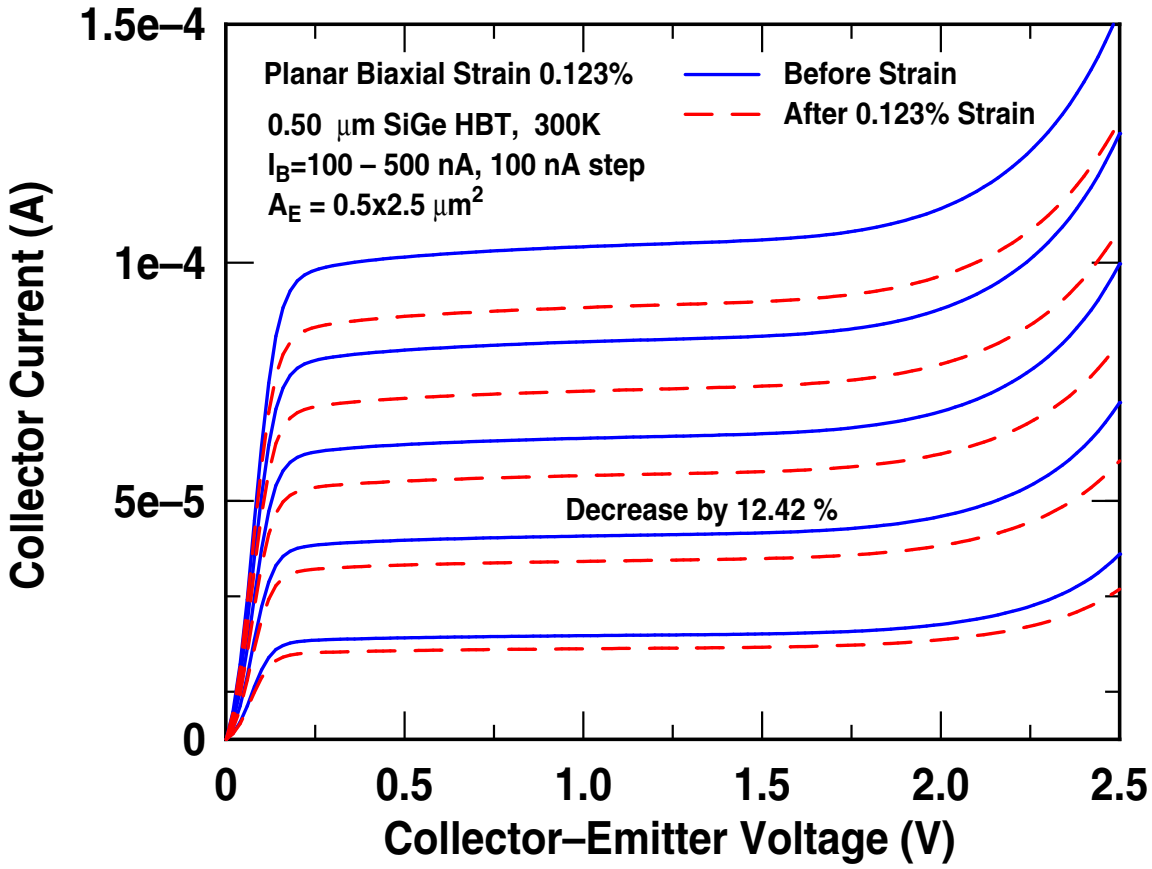

Figure 29: Output characteristics of a first generation SiGe HBT for both pre-strain and post 0.123% biaxial strain.

technology generations show a decrease in current gain with strain. Figure 31 illustrates this reduction in current gain. This figure also illustrates the higher current gain of 5HP SiGe HBTs over 5HP Si BJT, and also the larger current gain of 7HP SiGe HBTs than 5HP SiGe HBT technology.

Table 3 summarizes the percentage changes in the collector current, the base current and the current gain across three technologies after biaxial planar strain is applied. Figure 32 shows these changes graphically.

4.5.2 Discussion

In an attempt to explain the collector current (I_C) degradation after strain, the collector current equation (10), and the saturation current (I_S) relation (8) provide some insight.

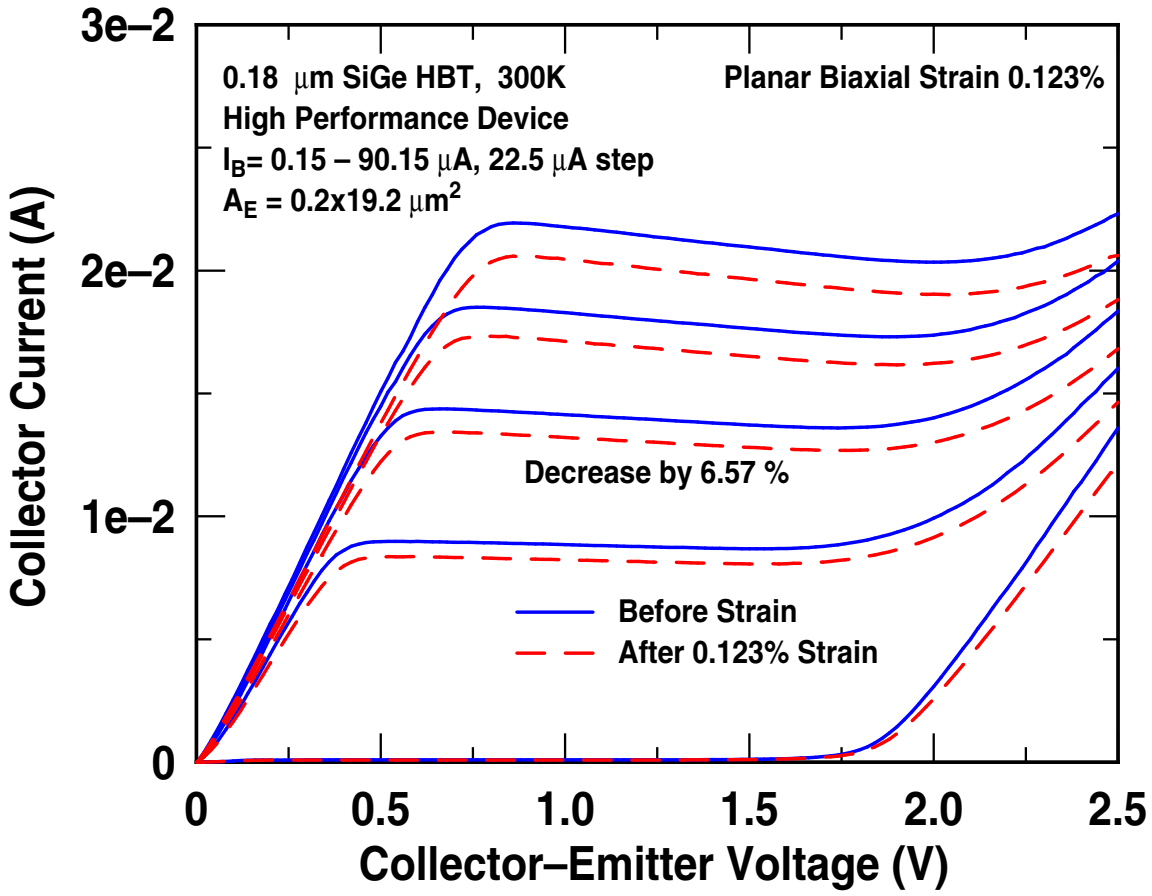

Figure 30: Output characteristics of a second generation high performance SiGe HBT for both pre-strain and post 0.123% biaxial strain.

The identical characterization environment for the pre and post strain devices confirm that the parameters that may change after strain are the minority electron mobility (μ_n) and intrinsic carrier concentration (n_{io}^2). Any decrease in minority carrier electron mobility will reduce saturation current and in turn collector current. The observed decrease in collector current in the strained devices, thus can in part be explained by the higher out-of-plane or longitudinal effective mass in the [001] valley (see Figure 20), that translates to reduced mobility. Unlike for MOSFETs, where carrier transport is parallel to the plane of the wafer or die, the carrier transport in BJT/HBTs is vertical to the plane. Therefore, the direction of electron transport in BJT/HBT is normal to the applied biaxial tensile strain. The applied strain increases the energies in the [010] and [100] valleys, and lowers the energy in the

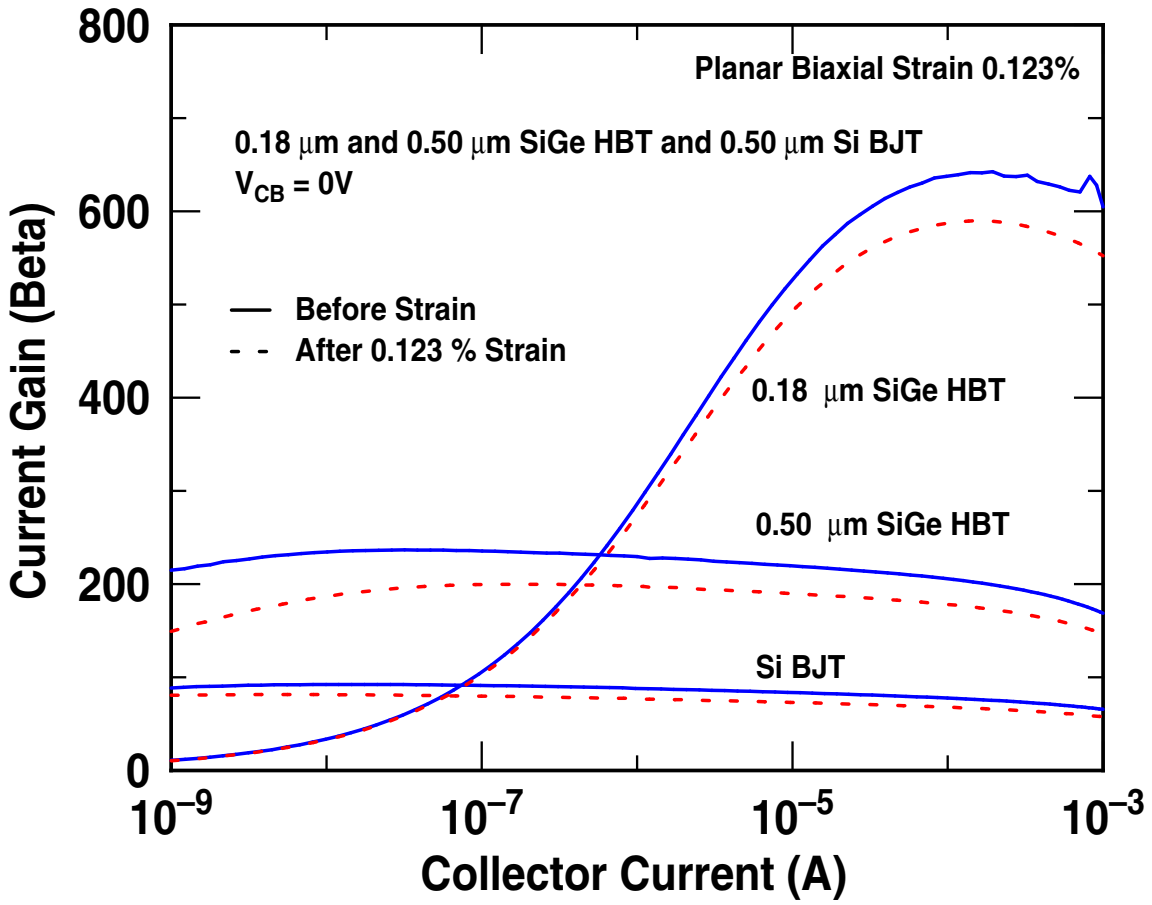

Figure 31: Current gain as a function of collector current for Si BJT and SiGe HBT.

[001] valley [68]. Electron transport is confined to the [001] valley due to the lower energy required. However, these electrons have a higher effective mass (0.91 m_0) in the direction of electron transport in the BJT/HBT, producing a reduction in the collector current. Another possible contributing cause of the observed decrease in the collector current is compressive strain in the orthogonal plane. Biaxial tensile strain causes compression normal to the strain plane. This compressive strain is about 1/3 of the applied tensile strain [34]. It is known that compressive strain generally degrades electron transport [35], and as a result, collector current in both the Si and SiGe devices decrease after strain.

It was discussed in chapter II that the compressive strain in SiGe HBT reduces the bandgap ((Figure 8). It can be expected that tensile strain will do the opposite, enhance the bandgap, and similar result is reported in literature as well [14]. Any increase in the

Table 3: Percentage change in collector current, base current and current gain across different technologies for biaxial strain.

Device Technology & Geometry	Δ **I**$_C$ **from I**$_C$**-V**$_{CE}$	Δ **I**$_C$ **from I**$_C$**-V**$_{BE}$	Δ **I**$_B$ **from I**$_C$**-V**$_{BE}$	$\Delta\ \beta$ **from I**$_C$**-V**$_{BE}$
0.50 μm Si BJT 0.5x2.5 μm^2	-12.35 %	-16.37 %	-6.84 %	-10.23 %
0.50 μm SiGe HBT 0.5x2.5 μm^2	-12.42 %	-9.12 %	5.13 %	-13.55 %
0.18 μm SiGe HBT 0.2x19.2 μm^2	-6.57 %	-2.05 %	5.76 %	-7.39 %

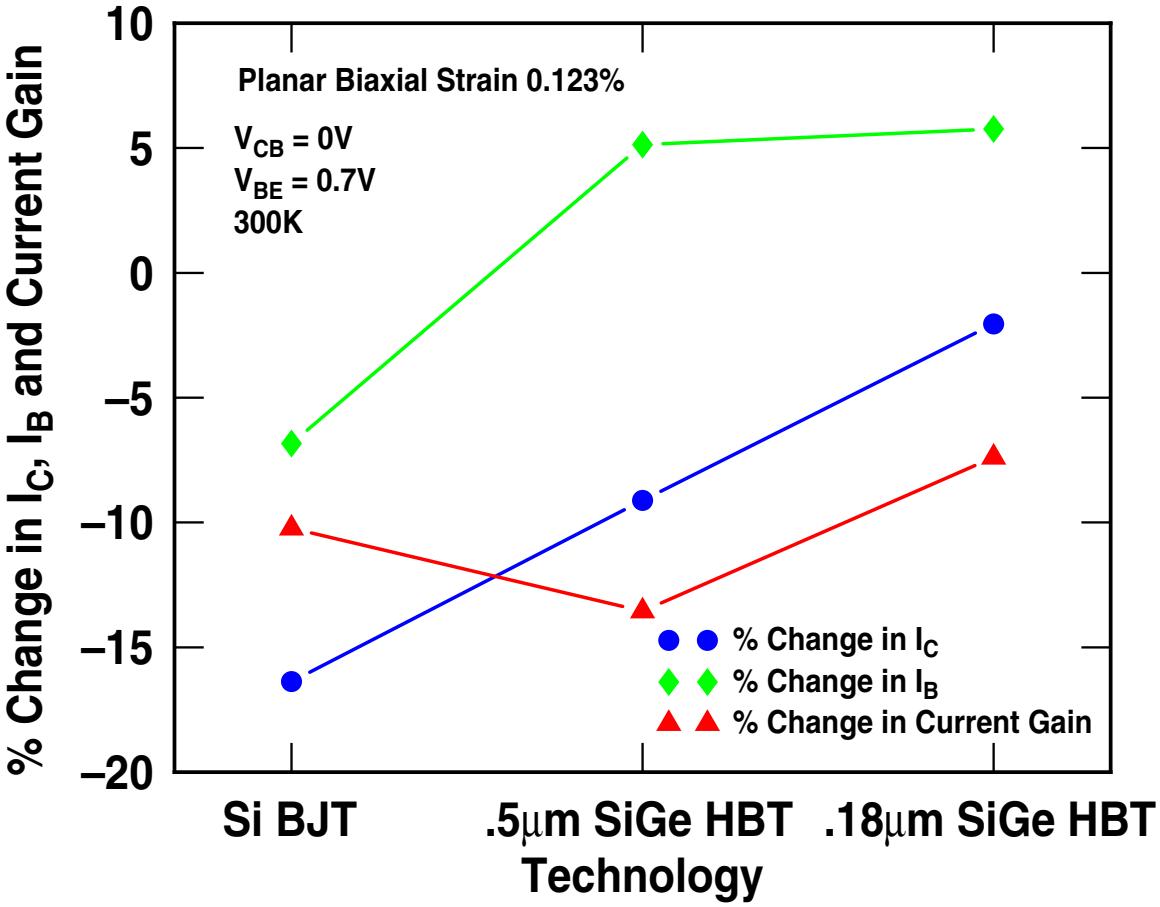

Figure 32: % Change in collector current, base current and current gain across different technologies.

bandgap will create additional potential barrier for electrons to be injected from the emitter to the base. This translates to a reduction in the emitter injection efficiency, and a degradation in collector current for the same applied V_{BE}.

From a first order analysis, if we assume that $N_C N_V$ does not significantly change after strain, the intrinsic carrier concentration (n_{io}^2) largely depends on $e^{-E_{go}/kT}$. An increase in bandgap, due to the applied tensile mechanical strain, will cause the intrinsic carrier concentration to go down, and thus alleviate saturation or collector current.

It is known that tensile strain applied in the two perpendicular or normal directions of current flow enhances hole mobility [36]. The base current in a BJT or SiGe HBT is mostly due to the holes injected from the base into the emitter, and the biaxial tensile strain tends to increase the mobility of these holes in the out-of-plane direction. The observed increase in the base current in the SiGe devices may be attributed to this phenomenon. We expected the base current for Si BJT devices to increase as well [14]. However, the experimental results exhibit a decrease in the base current for Si BJT devices, and is open for further investigation.

4.5.3 Dynamic Characteristics

The pre- and post-strain *ac* small-signal characteristics (f_T and r_{BB}) of two first-generation SiGe HBTs (0.5x1.0μm^2 and 0.5x2.5μm^2) are shown in Figure 33 and Figure 34 respectively. Both f_T and r_{BB} apparently decrease after strain (the latter expected due to the strain-induced improvement in the lateral hole mobility), but this change is small and within bounds of repeatability of the S-parameter measurements. Similar results were observed for different device geometries. For a through comparison, *ac* small-signal characteristics (f_T and r_{BB}) for a first generation Si BJT 0.5x2.5μm^2) is also included in Figure 35 Therefore, for this level of induced strain, no conclusive change in the *ac* small-signal characteristics is observed after strain is applied.

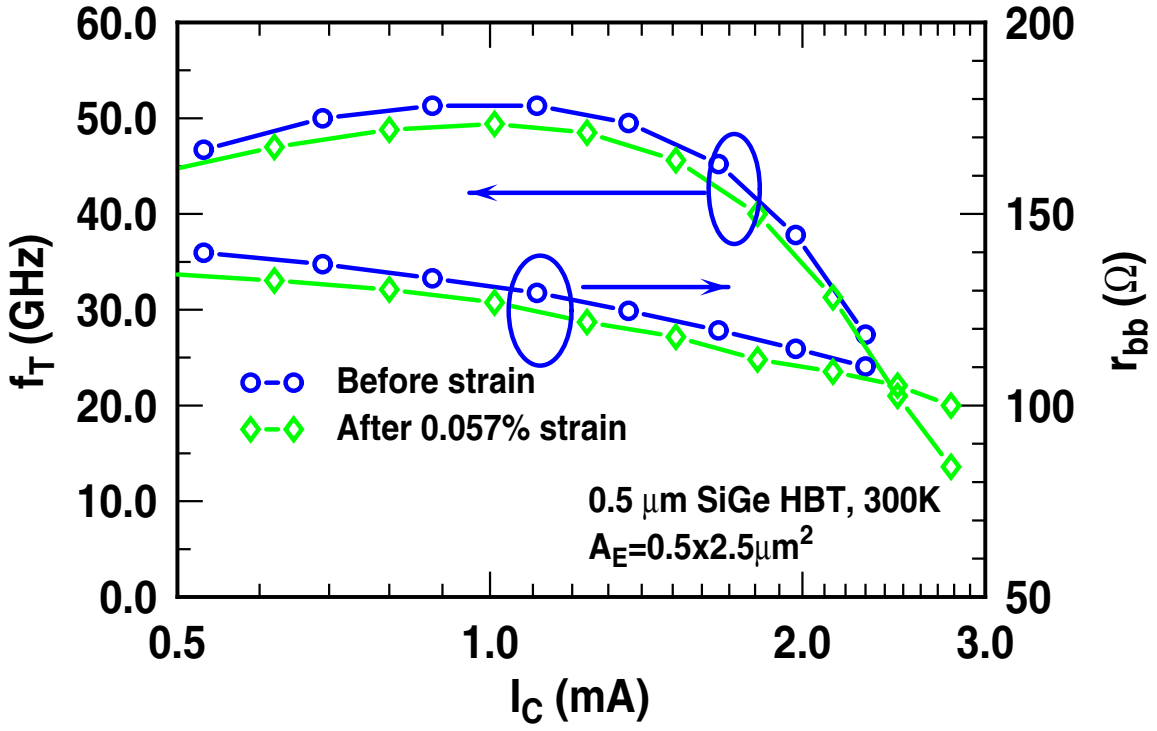

Figure 33: Pre-strain and post 0.057% strain f_T and r_{BB} of a first-generation SiGe HBT.

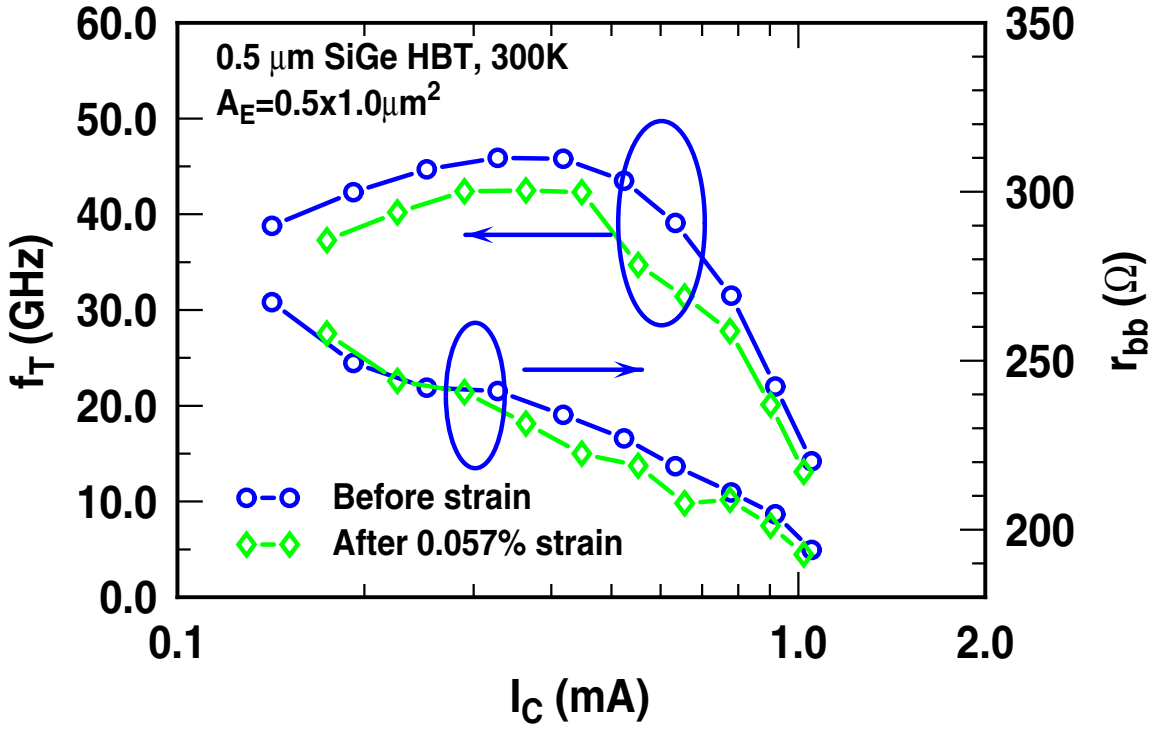

Figure 34: Pre-strain and post 0.057% strain f_T and r_{BB} of a first-generation SiGe HBT.

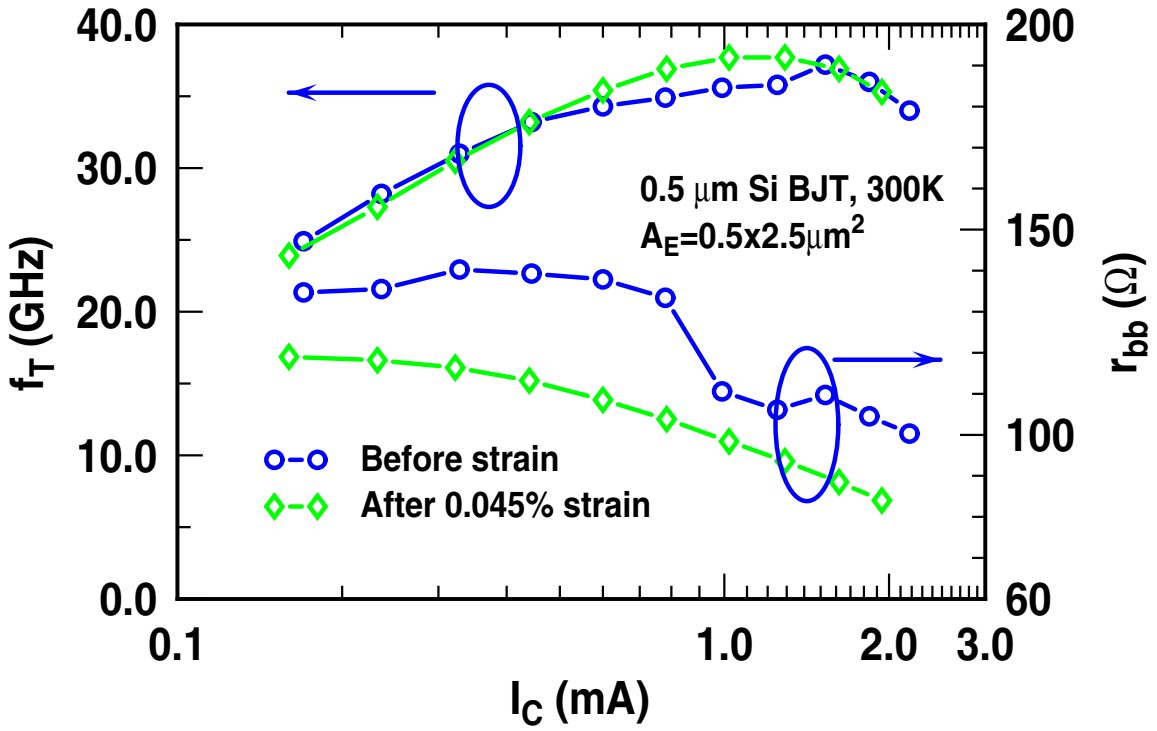

Figure 35: Pre-strain and post 0.045% strain f_T and r_{BB} of a first-generation Si BJT.

4.6 Uniaxial Strain Results

The uniaxial strain results presented in this section are based on the static characteristics of two different SiGe HBT technologies.

4.6.1 Static Characteristics

The before- and after-strain forward Gummel characteristics for the 7HP (0.18μm emitter length) high-performance SiGe HBTs (emitter area of 0.8x3.2μm^2) at 300K are shown in Figure 36. These SiGe HBTs show up to a 2.69% decrease in collector current (I_C) and a 4.68% increase in base current (I_B) at V_{BE} = 0.7V after strain, and is repeatable across multiple devices. The 0.18μm high-breakdown SiGe HBTs (emitter area 0.8x3.2μm^2) exhibit up to 4.63% decrease in I_C and 1.69% increase in I_B (Figure 37) after strain at the same V_{BE}.

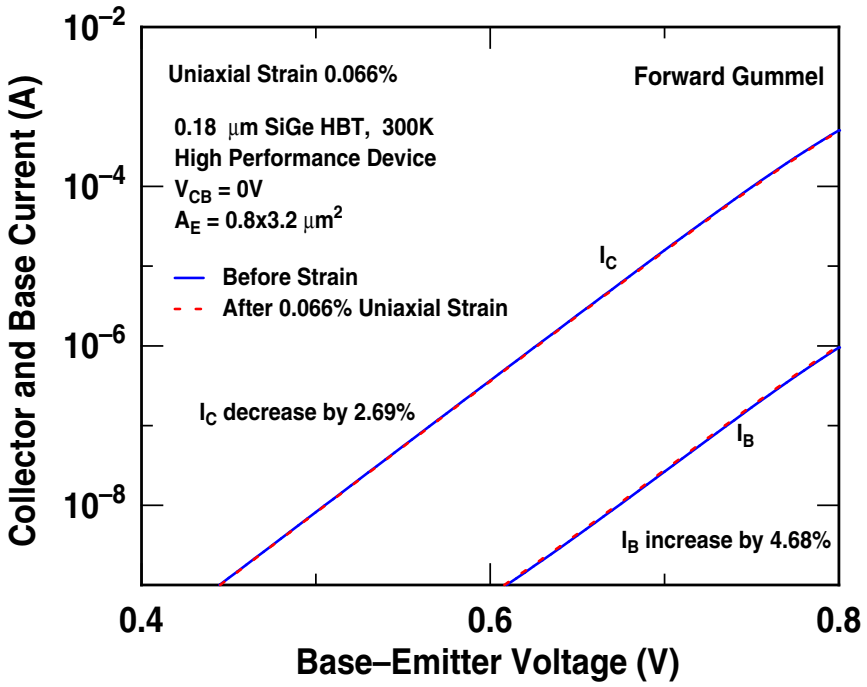

Figure 36: Pre-strain and post 0.066% uniaxial strain forward Gummel characteristics of a 2nd-generation high-performance SiGe HBT.

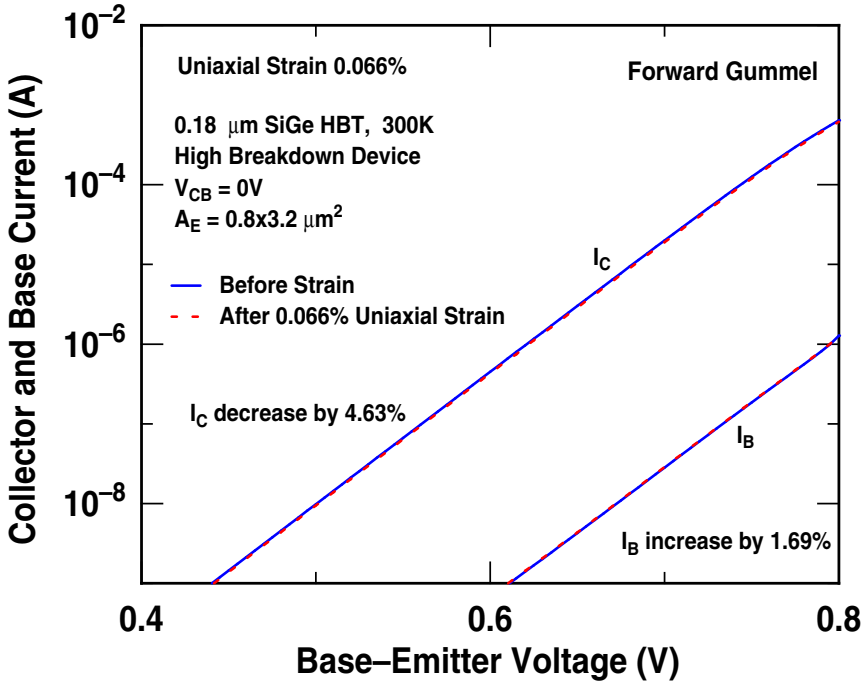

Figure 37: Pre-strain and post 0.066% uniaxial strain forward Gummel characteristics of a 2nd-generation high-breakdown SiGe HBT.

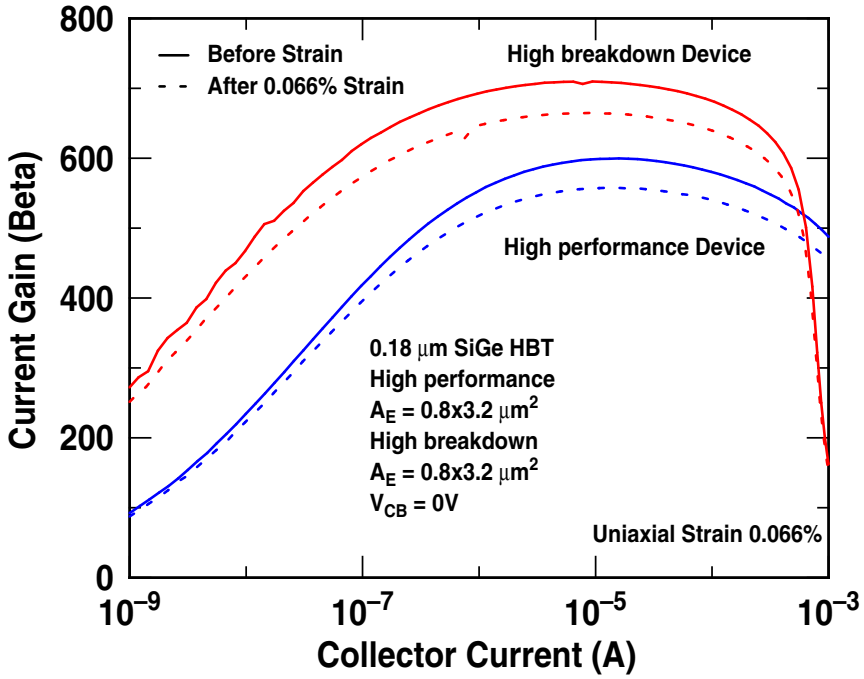

Figure 38: Current gain as a function of collector current for the second-generation SiGe HBTs.

Since the base current increases and the collector current decreases for both the high-performance and high-breakdown SiGe HBTs, the current gain degrades (decreases) after strain, and this reduction in the current gain is shown explicitly in Figure 38.

4.6.2 Discussion

The uniaxially strained SiGe HBT devices show similar trends as biaxial devices. However, an increase in collector current was expected. If strain is applied uniaxially, for instance along [010] valley or X direction (see Figure 20), the energy in this valley will be elevated, while the energies in the [001] and [100] valleys (Y and Z) are decreased [68]. Due to the lower energy required, electron transport will be then limited to the [001] and [100] valleys. The electrons in the [001] valley have a higher effective mass (0.91 m_0) in the direction of electron transport in the HBT, but the [100] valley electrons have a lower effective mass (0.19 m_0) in the same direction. These [100] valley electrons will dominate the electron transport over the [001] valley electrons, and due to their lower out-of-plane effective mass

or higher mobility, will produce an increase in the collector current. This is opposite to the biaxial strain case, where [001] valley electrons, due to their higher effective mass in the electron transport direction, reduces the collector current [13].

The above explanation, however is suitable when strain is applied along or parallel to one of the in-plane axes (either [100] or [010]) of the cubic structure of Si, and needs to be further examined. For this experiment, strain was not applied precisely in these directions. The wafer notch for these wafers were along the <110> axis, and tensile uniaxial strain was applied in this direction. This essentially implies that the uniaxial strain application was between the two in plane axes, namely [100] or [010], and the strain has components along both of these axes. Roughly, these components are about one half of the original strain, and most importantly becomes biaxial in nature [34]. Therefore, it is not surprising that similar behavior is replicated in the uniaxially strained devices. However, the amount of uniaxial strain applied is small compared to the biaxial strain, and due to the distributive effect along the cubic axes, it becomes even lesser. The low level change in I_C and I_B for the uniaxial samples may be explained due to low level of strain.

MOS devices show significant performance difference for different orientations of strain, since the carriers flow along the plane of the wafer. Due to carrier transport in vertical direction in BJT and HBT, uniaxial strain and biaxial strain may have less dramatic impact difference.

4.7 Summary

This chapter explains the overall experimental methodology, and the the results obtained. Possible explanation for the results have also been provided. In general, it is observed that biaxial tensile strain decreases I_C and increases I_B for SiGe HBT devices across two different technologies. However, Si BJT show a decrease in I_B. The dynamic characteristics, showed negligible change due to strain application. Uniaxially strained samples for the SiGe devices showed similar results as the biaxially strained devices. Current gain was

lowered in both biaxial and uniaxial types of straining techniques.

CHAPTER V

CONCLUSION

5.1 Conclusion

The effects of mechanical planar biaxial tensile strain applied, post fabrication, to Si/SiGe HBT Devices, has been examines. This work differs from other strain effect investigations in the fact that this particular mechanical straining technique was applied, for the first time on BJT/HBT. The collector current is reduced in all three technologies after strain. The Si BJTs demonstrate a decrease in base current while the SiGe HBTs exhibit an increase in base current. The *ac* small-signal results showed no significant change after strain. Also the effect of uniaxial strain on SiGe HBTs have been examined. The results suggest that this method of strain yields similar results as the biaxial strain. This was, however due the the specific direction of uniaxial strain. Uniaxial strain applied in proper direction may cause different results.

5.2 Future Paths

This experiment compares the effects of biaxial and uniaxial strain on Si bipolar and SiGe heterojunction bipolar devices, however only tensile strain, applied in a very particular way, has been investigated. It would be worth exploring the effects of strain on bipolar/heterojunction bipolar devices using local, as well global techniques, and how that compares with mechanical strain application. Investigation for new ways of strain application can also be inquired. Based on the discussions in Chapter IV, performance can be improved in BJT/HBT with the application of compressive strain. Compressive strain effects on bipolar/heterojunction bipolar devices has been examined [14] by mechanical bending

of wafers only, but other techniques are still open for further research. One other very interesting future direction would be to quantify the changes in BJT/HBTs with different levels of applied strain. Therefore, it is obvious that several different research attempts can be made regarding strain effects on BJT/HBT. A proper understanding of different phenomena about strain and BJT/HBT, can help creating better devices.

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